analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Low-Cost, High-Performance, Compact New Isolation Amplifiers (page 3)
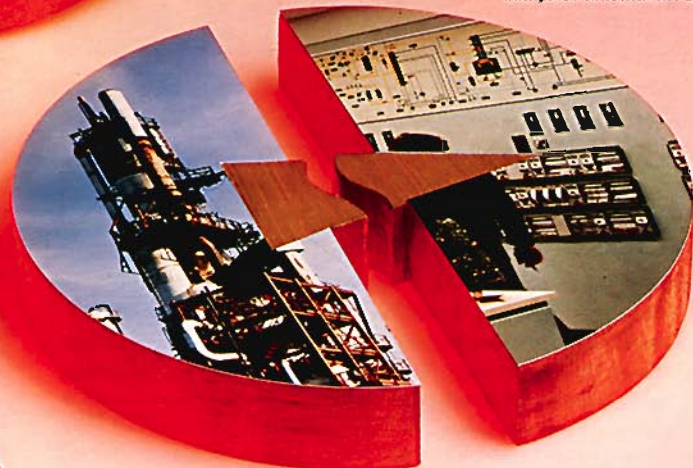Complete Monolithic µP-Compatible 5-µs, 12-Bit CMOS ADC in 0.3″ DIP (page 6)
Fast 64-Bit IEEE-754 Floating-Point Multiplier and ALU (page 7)
Monolithic AD574A Available in Plastic or Ceramic (page 24)
Complete Contents on Page 3

Low Cost

High Performance

ANALOG
DEVICES
AD204
ISOLATION AMPLIFIER
MADE IN U.S.A.   8531

Actual   Size

ANALOG
DEVICES

Volume 20, Number 1, 1986

Editor's Notes

ANALOG & DIGITAL

Bidecennial

If you noticed that this issue of *Analog Dialogue* is the first in Volume 20, you might have surmised that we're in our 20th year of publication—and you'd be right. For some reason, it's a human characteristic to reminisce on the occasion of round-number anniversaries. Although this Editor is a relative latecomer—having started with Volume 3 (this gives us the opportunity for another bidecennial celebration 2 years from now!)—it seemed appropriate to celebrate the 20th by comparing this issue with our first issue, Volume 1, Number 1—datelined Cambridge—in April, 1967 (now out of print). Here is the table of contents for that issue's 12 pages:

The by-lined authors in that issue were R. M. Gitlin, Bill Miller, and Ray Stata. It's interesting to note that our isolation amplifiers, ADCs & DACs, bipolar and CMOS ICs, laser wafer-trimming, DSP chips, MACSYM, RTI microcomputer interface boards (and microcomputers, too!), and—in fact—all our ICs, hybrids, and system products lay in the future. And so too were such addresses as Norwood, Wilmington, Limerick, East Molesey, Greensboro, Tokyo, and a host of other locations around the world that now are graced by the Analog Devices logo.

Of the products introduced in that issue, the model 180 op amp continues to be mentioned in the *1984 Databook*, listed among products "still available," and the orders keep coming in. In its prime, it was one of our big winners; for example, in 1971, the 180 enjoyed bookings near $0.5 million per year (about 4% of that year's business).

Digital Signal-Processing Progress

1986 marks substantial progress in Analog's mastery of the digital sector of this analog world. In this issue, we introduce 64-bit floating-point multipliers and ALUs, as well as "word-slice" building blocks of microcoded digital signal processors, and new-generation versions of standard multipliers and MACs with 1.5-μm CMOS geometries for higher speed, lower cost, and low dissipation. By the time you read these words, you may have already seen articles in the trade press introducing our single-chip digital signal processor. Analog's digital revolution rolls on! ▶

Dan Sheingold

ADI AUTHORS

Bill Windsor (page 7) is a Marketing Specialist in the Analog Devices Digital Signal-Processing Division. Before joining ADI, he worked at Honeywell's Small Systems and Terminals Division, designing custom minicomputer hardware. Bill holds a BSEE degree from M.I.T. and an MBA from the Harvard Business School. His spare-time activities include running, ski touring, and astronomy.

Paschal Minogue (page 14) is a Senior Design Engineer at Analog Devices, B.V., in Limerick, Ireland. He was graduated from University College, Dublin, with a Bachelor of Electronic Engineering degree in 1981. Before joining ADBV, and while still an undergraduate of U.C.D., he worked for two summers in a circuit research/design group at G.T.E., in San Carlos, California.
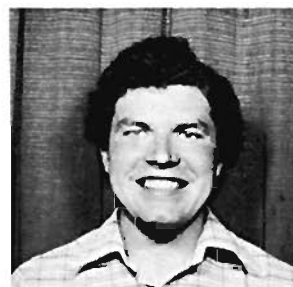
Bill Gotschewski (page 14) is a Marketing Engineer in the Microelectronics Division of Analog Devices. He was born in Glenview, Illinois and received his BSEE at the University of Illinois, Urbana-Champaign. Before joining Analog Devices, he designed high-speed analog hybrids and temperature-compensating circuitry used in conjunction with the products of Microwave Associates, Inc. (MA/COM). He enjoys basketball, softball, skiing, and camping.

David Fair (pages 7 & 10) is a Marketing Specialist in the DSP Division at Analog Devices. He has a BA in physics from Pomona College (Claremont, CA) and Ph.D. in the philosophy of mathematics, logic, and physics from Princeton University. Before joining ADI, he worked at the Strategic Planning Institute, in Cambridge, MA, and taught at the University of Vermont, Burlington. David's leisure-time activities include hiking, cycling, jogging, and windsurfing.

ISOLATION AMPLIFIERS BECOME LOW-COST COMPONENTS
High-Performance, Compact Alternative to User Circuit Development
AD202 & AD204 Use Surface-Mount Technology, New Circuit & Component Designs

by James Conant

The AD202 and AD204* are the first members of a revolutionary new generation of small, cost-effective isolation amplifiers, using automated assembly of surface-mounted components in a single-in-line-type package. Each amplifier is housed in a 1/4"-wide package, giving 4 channels of isolation per board inch. Within the small package, they act as full-function self-contained isolators, for both signals and power, with galvanic (transformer) isolation. Protecting people and equipment, they also preserve signal integrity.

Their small size and low cost are combined with high performance: ±1,000-volt peak-continuous isolation, 130-dB common-mode rejection, gain nonlinearity of ±0.025% (0.05% max) and gain drift of ±20ppm/°C (45 max). The AD202 stands alone, powered by a single +15-volt supply; the AD204 is for system applications of several or many (up to 32 or more) isolators, driven in synchronism by an AD246 Clock Driver. Prices (100s): $28/$25 (AD202JY/204JY).

Typical applications for these devices are in multi-channel data acquisition, current-shunt measurements, motor controls, process signal isolation, and instrumentation applications where high common-mode voltages are present. Their low cost and small space requirements may bring to mind many more new applications where isolation amplifiers were not likely to be considered in the past.

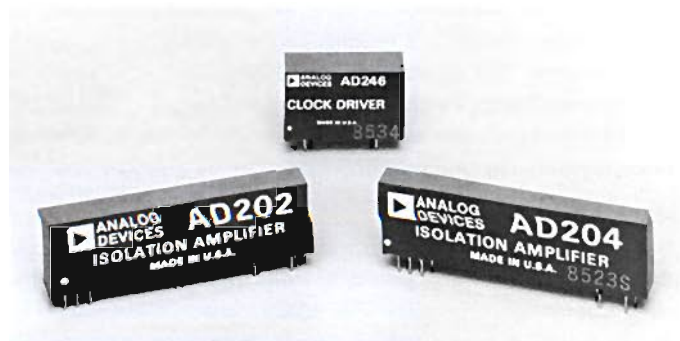## ISOLATION AMPLIFIERS ARE NOW COMPONENTS

Not so long ago, isolation amplifiers were big and power-hungry, with limited performance or flexibility. Design objectives for subsequent device families were to either maximize attributes or minimize cost. Models AD293/AD294 and AD295 exemplify the former, with improvements of size, performance, and flexibility. The AD202/204 represent the highest stage of the latter approach, a low-cost isolation amplifier that performs considerably better than its forebears. Table 1 is a history of ADI's low-cost isolators.

Automated assembly of surface-mounted components, the best technique short of monolithic (which has yet to be achieved with the mix of components used in transformer-isolated amplifiers), has dramatically reduced manufacturing cost and product size. The cost-breakthrough products, AD202 & AD204, are the result of this new technology, combined with a new circuit design. In ad-

dition to improved cost-size-performance, the new manufacturing technology takes advantage of automated testing, yield reporting, and built-in quality checks to provide major advances in product reliability.

WHY ISOLATION AMPLIFIERS?

Instrumentation design engineers have long been challenged to measure signals accurately in noisy industrial environments, where ground loops, ground disturbances and transients are commonplace. A feasible approach is to use instrumentation amplifiers (e.g., the AD625). They provide good common-mode rejection (CMR), low drift, and excellent linearity. However, they need a direct or implicit connection between signal and power common

Table 1. Evolution of isolation amps designed for low cost.

| SPECIFICATION	1971	1977	1985 (AD204)
Gain Nonlinearity	±0.2%	±0.05%	±0.025%
Gain vs. Temperature	±300ppm/°C	±200ppm/°C	±45ppm/°C
Offset Voltage	±50mV	±50mV	±20mV
Offset Voltage vs. Temperature	±150μV/°C	±100μV/°C	±20μV/°C
Power Consumption	225mW	175mW	35mW
Full-Power Bandwidth	200Hz	900Hz	5kHz
Weight (Ounces)	11.2	1.6	0.35
(Grams)	320.0	46.0	9.90
Size (Inches)	3.5 × 2.5 × 1.3	1.5 × 1.5 × 0.62	2.08 × 0.249 × 0.625
(Millimeters)	85 × 64 × 33	38 × 38 × 16	52.8 × 6.3 × 15.9
Price	$100	$50	$25

*Use the reply card for technical data.

Cover design by Shelley Cohane; photographs courtesy of Hewlett-Packard Company, Stock Boston, and Total Graphics.

for input bias-current return. This required connection can allow ground disturbances to severely degrade measurement accuracy. Perhaps as seriously, the supply rating limits their common-mode range. If input common-mode ratings are exceeded, damage can result—not only to the in-amp, but also to more-expensive components in the following stages.†

Unlike in-amps, isolation amplifiers have a fully floating front end (galvanically isolated—no conductive connection), which requires zero net bias current and permits two-wire-only connections to signal sources. This eliminates ground loops and other common-mode error sources. Furthermore, low-level signals riding on high CMV levels (hundreds—or thousands—of volts) can be easily and safely measured by isolation amplifiers.

HOW IT WORKS

A modulated-carrier isolation technique, with transformer coupling, is used to transfer power to—and signals between—input and output stages (Figure 1). The AD202 is powered by a +15V dc supply, which operates the internal carrier-drive oscillator. The AD204, designed for multichannel applications, is driven by an external clock driver, AD246, or a user-supplied clock.
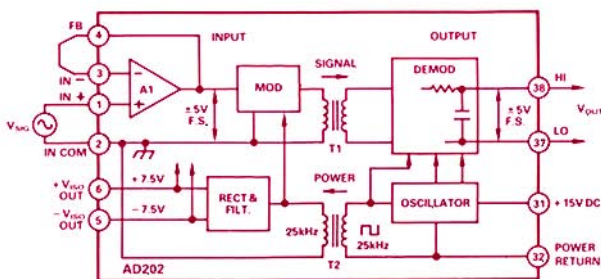
a. AD202 dc-powered isolator.
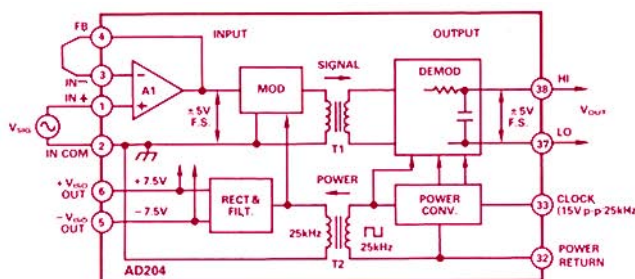
b. AD204 clock-powered isolator.

Figure 1. Functional block diagrams.

The AD202 generates a 25kHz signal, which serves as a power source and carrier; rectified and filtered, it provides a bipolar power source for the DEMODulator in the OUTPUT section. The ac signal is also transferred by T2 to the INPUT stage, rectified, and filtered to provide a second bipolar power source. This isolated supply powers the MODulator and the input amplifier, A1; in addition, dc power is made available at $\pm V_{ISO}$ pins 5 & 6 for external use in front-end preamps, sensor excitation, offsetting and trimming, etc.

†For information on isolation amplifiers, see the *Transducer Interfacing Handbook*, Analog Devices, 1980 ($14.50), and the free "Applications Guide for Isolation Amplifiers and Signal Conditioners."

The output signal from A1 modulates the 25kHz signal, which—serving as a carrier—transfers the input-signal information across T1. The received signal is then demodulated at the OUTPUT stage, thus reproducing the original signal from A1.

ALTERNATIVES: MAKE vs. BUY

Until now, the cost of packaged isolation amplifiers has been considered to be high enough so that, for many applications requiring isolation, users chose to design and build (instead of buying) isolation circuitry. Although providing basic isolation, this approach all-too-often sacrifices performance, reliability, or size for low cost. Two of the most-common approaches to low-cost isolation for in-house designs are optically coupled voltage-to-frequency converters and flying-capacitor relays.

Optically coupled isolation amplifiers were also marketed as an alternative low-cost commercial approach. However, this solution offered only minimal performance, having excessive (for many applications) drift with time and temperature. In addition, the isolation technique requires the use of an external DC/DC converter, which adds circuit complexity and vitiates the purported size and cost advantages of the isolator by itself.

The AD202/204 offer a true alternative to in-house isolation techniques, without compromising performance, reliability or size; they also provide performance advantages that overshadow today's commercially available optically coupled devices. Table 2 compares characteristics of the AD202/204 and popular isolation techniques. The key specifications for both models are summarized in the box.

Table 2. Comparison with other approaches.

Character-istic	AD204/AD202	Flying-Capacitor Relay[1]	Optically Coupled Converters	Commercial Optical Iso-Amps
CMV Rating	Excellent (1,000 V pk)	300 V to 600 V (relay dependent)	Good-Excellent[2]	Good-Excellent (750 V pk)
CMR Rating	Excellent (>130 dB)	Excellent (>130 dB)	Excellent (>120 dB)	Excellent (>120 dB)
Linearity	Good (±0.025%)	Excellent (with best relay & capacitor)	Fair-Good (converter-dependent)	Fair-Good
Bandwidth	Good (5/1.5 kHz)	Poor (low-frequency)	Poor (VFC); Good (successive approx.)	Good (5 kHz)
Temperature Stability	Good	Excellent (with best relay)	Good	Poor
Time Stability	Excellent	Excellent (with best relay)	Excellent	Poor
Power Consumption	Excellent (35/70mW)	Fair (requires coil drive)	Fair (extra DC/DC converter required)	Fair (separate dc-dc converter)
Reliability	Excellent	Fair (relay maintenance)	Excellent	Good
Application Versatility	Excellent	Poor (limited applications)	Excellent (depends on converter)	Excellent
Price Per Channel[3]	$25/$28	$20-$30 (plus support circuitry)	$35-$70 (depends on converter)	$35-$60

Notes
[1]Mercury-wetted-contact relays required to obtain the best performance, but they are sensitive to position. Reed relay's performance degrades with sustained common-mode stress.
[2]CMV rating depends on rating of both optical coupler and DC/DC converter.
[3]Price per channel will vary according to total channel count and required performance limits.

The input amplifier of the AD202/204 is an uncommitted op amp; the user can tailor its performance to meet the application need—including functional configurations, amplifying, optional gain- and offset adjustments, and added filtering. Figure 2 illustrates basic input connections for inverting and noninverting amplification.
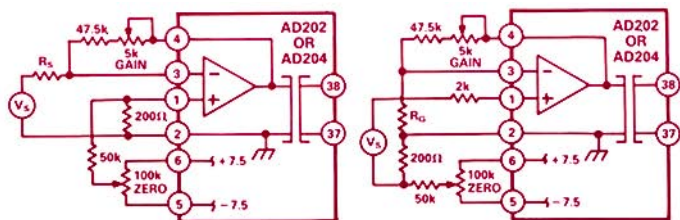
a. Inverting connection. b. Noninverting.

Figure 2. Op-amp connections, with zero and gain trims.

APPLICATIONS

In addition to basic isolation, the AD202/204 offers many design benefits for the user. Besides the uncommitted input amplifier, which can be configured as a buffer, or with gain up to 100V/V, isolated front-end output power is available (±7.5V @ 2mA – AD204), enough to operate a low-drift preamp or provide excitation for a semiconductor strain gage or other ancillary circuits. Some common applications of the AD202/204 are illustrated in Figures 3-5.

Low-Level Sensor Inputs The outputs of low-level sensors, such as thermocouples, can be isolated and signal-conditioned with the circuit shown in Figure 3. The isolated output power at pins 5 and 6 provides excitation for a low-drift input amplifier. In addition, a 3-pole active filter provides normal-mode rejection of frequencies above a few Hz, while enhancing common-mode rejection at 60Hz. For multi-channel applications, multiplex the outputs of an appropriate number of similar circuits, sharing the same clock source.
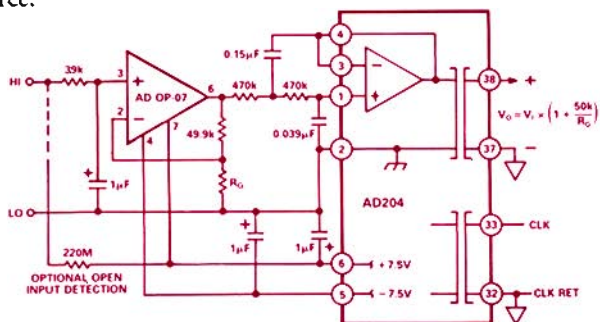

Figure 3. Preamplifier for low-level sensor input.

Process-Current Loop Receiver—Figure 4 shows one way to isolate and convert a 4-20 mA process signal to a 0-10-volt output range. A 250-ohm shunt resistor converts the 4-to-20 mA to a 1-to-5-volt signal. For a 0-to-4-volt output signal, a Zener diode produces a fixed offset of − 1V at pin 37, biasing the output appropriately with respect to ground. An external amplifier with 2.5 V/V gain scales the output to 0-10 V and also buffers the AD202/204 output. This circuit requires a loop with a (usually available) source compliance of at least 5V. For lower compliance levels, use less shunt resistance and scale the gain appropriately.
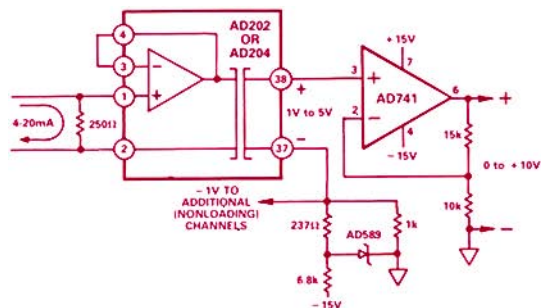

Figure 4. Process current-loop receiver application.

BASIC PERFORMANCE SPECIFICATIONS
(typical @ +25°C & V_S = +15V)

MODEL	AD204JY	AD202JY
GAIN		
Range	1 V/V to 100 V/V	
Error	± 0.5% typ. (± 4% max.)	
vs. Temperature	± 20 ppm/°C typ. (± 45 ppm/°C max.)	
Nonlinearity (G = 1V/V)	± 0.025% typ. (± 0.05% max.)	
INPUT VOLTAGE RATINGS		
Max. CMV Input to Output		
AC 60Hz, Continuous	750Vrms	
DC Continuous	± 1,000 V peak	
COMMON-MODE REJECTION		
R_S ≤ 100 ohms		
(HI & LO Inputs) G = 1	110 dB	105 dB
G = 100	130 dB	130 dB
LEAKAGE CURRENT, INPUT TO OUTPUT		
@ 240Vrms, 60Hz.	2 μA rms max.	
FREQUENCY RESPONSE		
Bandwidth		
V_O = 10V P-P, G = 1V/V to 50V/V	5 kHZ	1.5 kHZ
OFFSET VOLTAGE		
Initial, @ 25°C,		
Adjustable to Zero	(± 5 ± 15/G) mV max.	
vs. Temperature	(± 10 ± 10/G) μV/°C	
ISOLATED POWER OUTPUT		
Voltage, Full Load	± 7.5 V	
Accuracy	± 10%	
Current	2 mA	400 μV
Load Regulation	5%	
RATED OUTPUT		
Voltage	± 5 V	
Output Impedance	3 kΩ	7 kΩ
Output Ripple		
100kHz BW	10 mV p-p	
5kHz BW	0.5 mV rms	
POWER SUPPLY		
Voltage, Rated Performance	(SEE	+ 15 V ±5%
Operating	AD246)	+ 15 V ± 10%
Current, No Load		5mA
TEMPERATURE RANGE		
Rated Performance	0°C to + 70°C	
Operating	− 25°C to + 85°C	
Storage	− 25°C to + 85°C	
PACKAGE DIMENSIONS		
Inches	2.08 × 0.249 × 0.625	
Millimeters	52.8 × 6.3 × 15.9	
CLOCK DRIVER	**MODEL AD246JY**	
OUTPUT		
Frequency	25 kHz Nominal	
Voltage	15 V p-p Nominal	
Fanout	32 units max	
POWER SUPPLY REQUIREMENTS		
Input Voltage	+ 15 V ± 5%	
Supply Current		
Unloaded	3.5 mA	
Each AD204 adds	2.2 mA	

Motor-Control Isolator—Figure 5 illustrates the use of two isolation amplifiers to sense voltage and current in a dc motor-control application. Isolator A1 senses 1/100 of the armature voltage (i.e., 5 volts) and reads it out at unity gain. A2, sensing current with a 0.1-volt shunt, operates at a gain of 50V/V, which provides a 5-volt output proportional to the armature current. The AD204 can also be applied in ac motor controls, where rejection of fast common-mode steps and reasonable bandwidth are essential. ▶
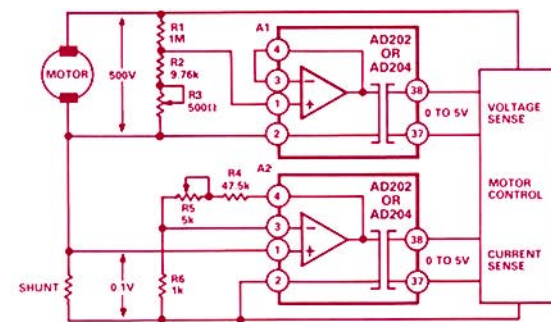

Figure 5. DC motor-control application.

MONOLITHIC CMOS A/D CONVERTER: 12 BITS IN 5 µs
AD7572 Has Buried Zener Reference, DAC, Comparator, S-A Circuitry, Latches
LC²MOS Process Results in Excellent Performance, Smaller Package (0.3" DIP)

The AD7572* is a complete true-12-bit a/d converter with both high speed (5-microsecond conversion time) and low power dissipation (165 mW maximum). It is fabricated in the Analog Devices linear-compatible CMOS (LC²MOS) process, an advanced, all ion-implanted process that combines fast CMOS logic and linear bipolar circuitry on a single chip; this means that it can achieve excellent analog performance while retaining the low power levels and high circuit packing density that are inherent in CMOS.

Because it uniquely combines high speed and resolution, compact package and low dissipation, functional completeness, and high-speed bus compatibility, the AD7572 is a true general-purpose a/d converter for 12-bit applications (no missing codes over temperature) at sampling rates up to 200 kHz. Telecommunications, sonar, and radar signal processing, as well as wideband data acquisition, are just a few of its typical application areas.

The AD7572 (Figure 1) uses an accurate high-speed DAC and comparator (employing wide-bandwidth PNP transistors) in a fast successive-approximation loop; its reference voltage is provided by a low-drift on-chip temperature-compensated buried Zener diode. The 12-bit parallel digital outputs may be multiplexed in two bytes (right-justified) for 8-bit buses or broadsided for 16-bit buses. Because of its fast interface timing (70-ns three-state enable and 25-ns bus-relinquish times), the AD7572 will operate with most popular microprocessors, including MC68000, TMS32010, 8085A, Z80.

A self-contained converter, it requires only power, control inputs, and the usual bypass capacitors. The on-chip clock circuit may be used with a crystal for stand-alone operation, or it may be driven from an external clock source, such as a divided-down microprocessor clock.

APPLICATION WITH S/H FOR BIPOLAR INPUT SWING
Figure 2 shows the analog connections for using the AD7572 with a high-speed sample/hold. The maximum sampling frequency is 125 kHz for 5-µs conversion, and 64.5 kHz for 12.5-µs conversion, including the 3-µs acquisition time of the AD585.

In addition to providing the track-hold function, the AD585 also drives the converter at low impedance; and a bipolar offset for a ±2.5-volt input range is added at the summing input, using the converter's own reference to provide the tracking offset voltage.

When the conversion is initiated, the converter $\overline{BUSY}$ input goes low, indicating that a conversion is in progress. The falling edge of the $\overline{BUSY}$ output signal places the sample-hold amplifier in Hold, freezing the input signal to the AD7572. When conversion is finished, the $\overline{BUSY}$ output returns High, allowing the sample/hold to track the input signal. At the maximum sampling rate, the AD7572's output data is read during the 3 µs immediately after conversion, while the sample/hold is acquiring the next sample. ▶
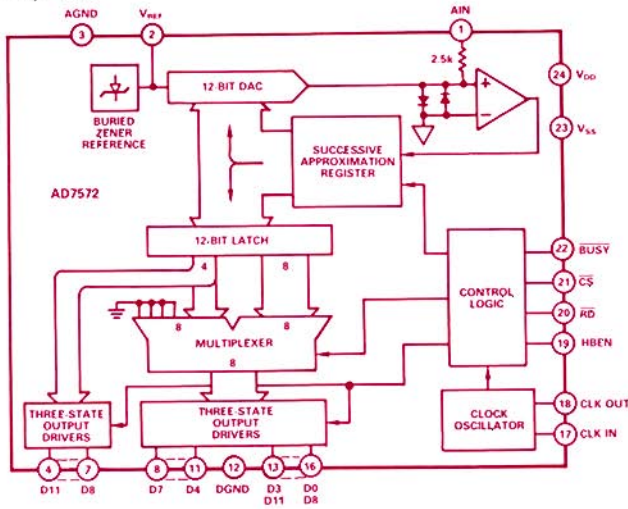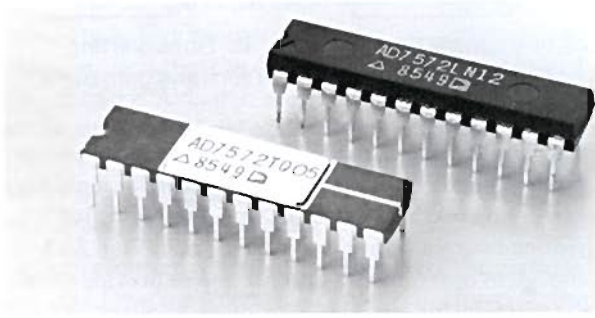

Figure 1. Functional block diagram.

It is available in a selection of performance grades, distinguished by full-scale temperature coefficient and nonlinearity (25 ppm/°C, 1/2 LSB); 50 ppm/°C, 1/2 LSB; and 50 ppm/°C, 1 LSB) for all popular temperature ranges, including −55°C to +125°C. A lower-cost 12.5-µs family—otherwise identical—is available for applications that require low power consumption and high accuracy but can tolerate somewhat lower throughput rates. Packaging includes 24-pin plastic, cerdip, and ceramic DIPs—and 28-terminal leadless chip carrier. Prices start at $46. in 100s, for the 5-µs version, and at $35. for the 12.5-µs version.

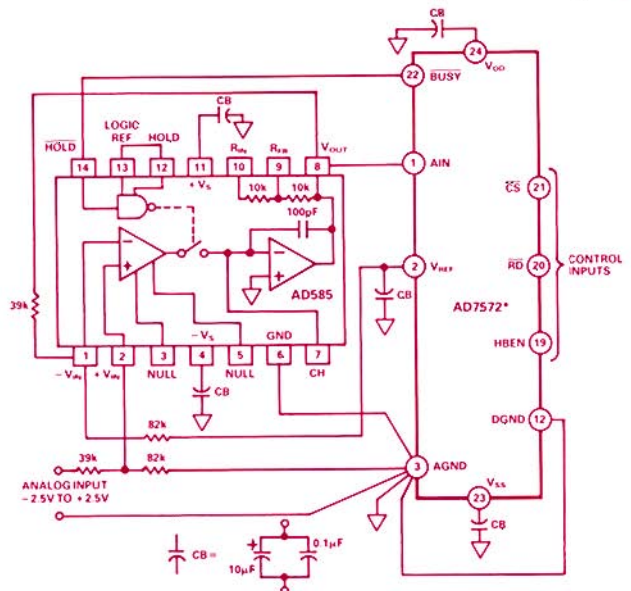*Use the reply card for technical data.

Figure 2. Application with sample/hold for 125-kHz throughput.

FAST 64-BIT IEEE-754 FLOATING-POINT MULTIPLIER AND ALU
ADSP-3210 & 3220 Handle 32-Bit Fixed and 32- or 64-Bit Floating Point
10-MFLOPS (100-ns) Single-Precision Throughput, Low-Dissipation (400 mW) CMOS

by Bill Windsor and David Fair

The CMOS ADSP-3210* Multiplier and ADSP-3220* ALU (Arithmetic & Logic Unit) form a floating-point chip set that contains the basic elements for implementing a high-speed 64-bit numerical processor, capable of performing floating-point arithmetic operations with a hitherto unavailable combination of high speed, low dissipation, and wide dynamic range, while maintaining compatibility with IEEE Standard 754 (draft 10.0) for binary floating-point arithmetic.

With these devices, all single-precision (SP) 32-bit and double-precision (DP) 64-bit floating-point arithmetic and logic operations—as well as 32-bit twos-complement fixed point—can be performed at 10 megaflops (million floating-point operations per second), with the exception of double-precision floating-point multiplication, which can be performed at 2.5 Mflops.

The availability of single- and double-precision floating point—and fixed-point—operations permits the ADSP-3210 and ADSP-3220 to be applied wherever dynamic range is critical or floating point calculations are necessary. Engineering-workstation and high-end personal-computer accelerators, mini-supercomputers, and array processors require the wide dynamic range of *double-precision floating-point operations* for such tasks as SPICE simulation and finite-element analysis; sonar, radar, and guidance systems typically demand the high-speed pipelined execution of *single-precision* operations; and graphic systems often employ 32-bit *fixed-point* arithmetic to calculate memory pointers for their pixel arrays.

FLOATING-POINT ARITHMETIC

Floating-point, or "scientific," notation is a computational convenience familiar to engineers and scientists. A floating-point number is expressed as the product of a "normalized" number (mantissa)—a mixed fractional expression, with a single non-zero digit to the left of the integer point—and a power of the number base. For example,

$$0.000000000003984_{10} = 3.984 \times 10^{-12}$$

$$0.0011011110_2 = 1.1011110 \times 2^{-3}$$

$$3F2.3E_{16} = 3.F23E \times 16^2$$

Floating point permits a data word with a given resolution to represent a wide dynamic range of quantities; in IEEE-754 (Draft 10.0) floating point, for example, the dynamic range available in 32-bit notation, for a normalized positive or negative binary number with a 24-bit mantissa, is from 2^{-126} to about 2^{+127}.

Multiplications are performed by multiplying the mantissas, adding the powers, and re-normalizing in case of overflow. For example,

$$6.2 \times 10^3 \cdot 2.3 \times 10^2 = 6.2 \times 2.3 \cdot 10^{(3+2)}$$
$$= 14.26 \times 10^5$$
$$= 1.426 \times 10^6$$
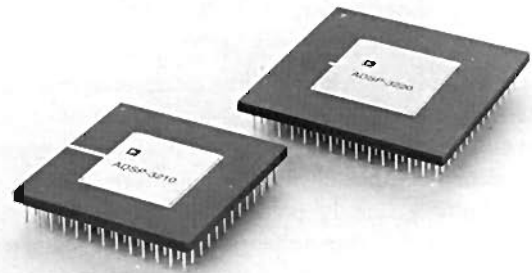
Addition is achieved by normalizing the number with the greater exponent to make both exponents equal, performing the operation, then re-normalizing in case of overflow.

$$9.3 \times 10^3 + 7.3 \times 10^2 = 93 \times 10^2 + 7.3 \times 10^2$$
$$= 100.3 \times 10^2$$
$$= 1.003 \times 10^4$$

In binary, these operations can be performed in the same way:

$$1.011 \times 2^3 \cdot 1.100 \times 2^2 = 10.0001 \times 2^5$$
$$1.00001 \times 2^6$$

$$1 \tfrac{3}{8} \times 2^3 \cdot 1 \tfrac{1}{2} \times 2^2 = (^{33}/_{16})(2^5)$$
$$= 2 \tfrac{1}{16} \times 2^5$$
$$= 1 \tfrac{1}{32} \times 2^6$$

In binary floating-point math (and the IEEE standard), the leftmost digit of a normalized mantissa is the integer, "1."; however, this is not universally adopted by computer manufacturers—in DEC systems, for example, binary floating-point numbers are normalized to 0.1.

Double Precision. For a computer bus having a given resolution, n, greater resolution and accuracy can be achieved by the use of "double precision," i.e., letting a pair of n-bit numbers, A and B, represent a 2n-bit number. The second number has an exponent which is *n* less than that of the first. For example, the fixed-point 8-bit number, 10111001, can be expressed as two 4-bit† numbers, A and B: 1011×2^4 and 1001. In floating point they would become 1.011×2^7 and 1.001×2^3.

Operations are performed with the number pairs, treated as sums. For example, two floating-point double-precision (DP) number pairs, (A + B) and (C + D), equal to $(A' \times 2^a + B' \times 2^{a-n})$ and $(C' \times 2^c + D' \times 2^{c-n})$, would have the sum (after normalizing to equalize the exponents),

$$(A + C) + (B + D)$$

which could be re-normalized as a pair of n-bit numbers. The *product* of the two 2n-bit numbers would be

$$(A + B)(C + D) = AC + AD + BC + BD$$
$$= A'C' \times 2^{a+c} + A'D' \times 2^{a+c-n}$$
$$+ B'C' \times 2^{a+c-n} + B'D' \times 2^{a+c-2n}$$

†Obviously, more bits are required for exponents and sign—"4-bit" here refers to the bits actually determining the mantissa's resolution.

*Use the reply card for technical data.

which can be re-normalized and rounded to a number of bits that depends on the desired resolution for the product. The need for four multiplications in DP accounts for the specified decrease of the ADSP-3210's multiplier throughput to 2.5 Mflops in DP from 10 Mflops for SP.

FLOATING-POINT STANDARDS

Floating-point standards are necessary in order that data words, controls and flags, arithmetic processes, and computational results be interpreted in the same way in all compatible software, equipment, and components.

Among the issues for which a common interpretation is necessary are: *data format* (single-precision 32-bit floating point, double-precision 64-bit floating point, etc.), *operand types* (denormalized numbers, signed zero, infinities, not-a-number (NAN)), *operations* (add, multiply, floating-point divide and square-root, quadrant normalizing for trigonometric functions, operations on denormals), *rounding modes* (to nearest number, toward plus infinity, minus infinity, zero), and the *handling of exceptions* (overflow, underflow, invalid operation, inexact result).

A number of sources of 32-bit floating-point standards exist. Among the best known, besides IEEE-754, are DEC, IBM/Data General, MIL-STD 1750, MIL-STD 1862B, and a host of others, including "home-brew" formulations established by users with special needs.

It was important, for the benefit of future designers of DSP systems, that Analog Devices adopt a standard that is likely to grow in popularity and widespread use. Accordingly, the floating-point operations of the ADSP-3210 and 3220 were designed to be compatible with IEEE Standard 754, now developing a growing momentum (its format is almost identical to MIL-STD 1862B).

In addition, in order to be maximally useful for 32-bit processing in many of the applications not needing floating-point operation, these devices include 32-bit fixed-point arithmetic in their repertoire. In this mode, besides performing computations with speed and simplicity, the user retains a full 32-bits of resolution (single-precision floating point has 24 bits of resolution, reserving 8 bits for the exponent).

The standard formats of IEEE-754 are:

Single-Precision 32-Bit Floating Point

Bit(s)	31	30 ------- 23	(.)	22 ------------- 0
Interpretation	sign bit	8 bits exponent field	implicit binary point	23 bits fraction portion of mantissa
		MSB LSB		MSB LSB
	s	e_7 ------- e_0		f_{22} ------------- f_0

The basic 32-bit format has a 24-bit signed-magnitude fraction and an 8-bit offset-binary exponent. Since the leftmost bit of the mantissa—in a normalized floating-point number—is a "1", it is omitted and serves as a "hidden bit"; only the fractional portion of the mantissa to the right of the binary point is represented. The "hidden bit" effectively increases the resolution of the mantissa by 1 bit; it also ensures—by definition—that all floating-point numbers are properly normalized.

The exponent is represented in offset binary, i.e., with a "bias" of +127, which must be subtracted from the value of the 8-bit exponent field. Thus, when the exponent representation in the number is 10000000 ($= 128_{10}$), the true exponent value is equal to

$128 - 127 = 1$; for an exponent value of zero, the exponent representation is 01111111. Valid exponents range from -126 ($= 00000001$) to $+127$ ($= 11111110$). 00000000 and 11111111 are reserved for special operands. In the normalized single-precision range, the value of the number is: $(-1)^s 2^{(e-127)} (1.f)$.

Double-Precision 64-Bit Floating Point

Bit(s)	63	62 ------ 52	(.)	51 ------------ 0
Interpretation	sign bit	11 bits exponent field	implicit binary point	52 bits fraction portion of mantissa
		MSB LSB		MSB LSB
	s	e_{10} ------- e_0		f_{51} ------------- f_0

In 64-bit words, the mantissa is expressed by 53 bits (52 bits plus the hidden "1.") and the exponent by 11 bits—with a bias of +1023. The value of a number is: $(-1)^s 2^{(e-1023)} (1.f)$, excluding $e = 0$ and $e = 2047$; this gives a range of usable exponents from +1023 to -1022.

In both of the above cases, the IEEE Standard provides for further extending the dynamic range, by as much as 2^{23} (SP), by allowing operations with *denormals*, numbers with a fixed exponent and a non-zero fraction (for example, 0.0011×2^{-126}). Denormals are used in "gradual underflow" to represent numbers of magnitude less than the minimum value representable in the normalized format. The exponent is set to its minimum value of -126 (SP) or -1022 (DP), and the hidden bit is 0. Denormal values are $(-1)^s 2^{-126} (0.f)$ in single precision and $(-1)^s 2^{-1022} (0.f)$ in double precision. They require special handling, because the arithmetic hardware must detect the reserved exponent value and insert a hidden bit of 0, as opposed to the hidden bit of 1 for the normalized number.

THE CHIPS

The ADSP-3210 Floating-Point Multiplier (Figure 1), housed in a 100-pin grid-array package, has a single 32-bit input port and a single output port for data, two pairs of multiplexed 32-bit input
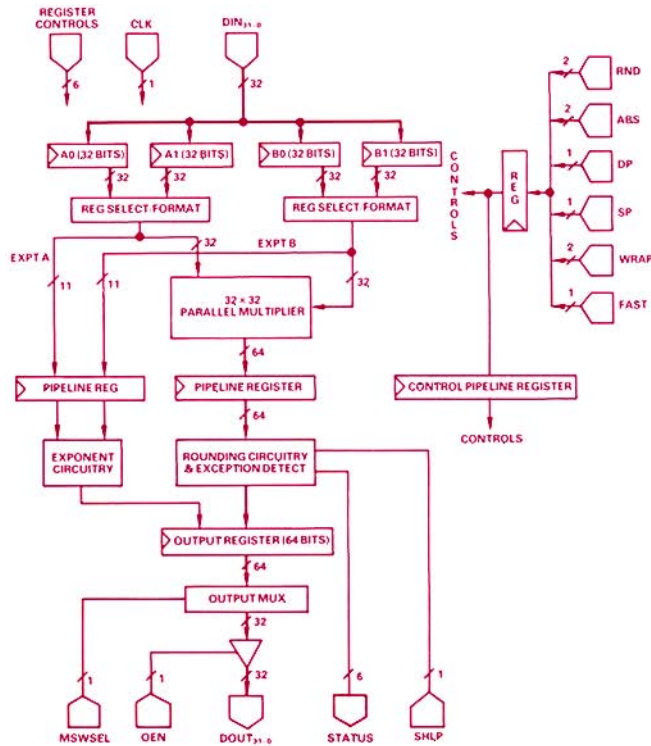

Figure 1. ADSP-3210 Floating-Point Multiplier.

registers and a 64-bit multiplexed output register, a 32×32 bit parallel multiplier, and control logic. A pipeline register stores the multiplier output while the output is formatted, then clocked into the output register.

Figure 2 shows the timing sequence for single-precision floating-point operations. Data latched in at the first 100-ns clock cycle is multiplied during the second clock cycle (while new data is latched in), formatted during the third clock cycle (while the new data is multiplied), and made available at the output during the fourth clock cycle (while the new data is formatted).

Thus, each new set of data follows the previous set by one clock cycle, or 100 nanoseconds, for a SP *pipelined throughput rate* (after the internal pipeline is filled) of 10 Mflops; The *scalar latency* (for one set of SP data) is 300ns, from input setup to valid output in Direct Operand Feed. Pipelined throughput is the key speed characteristic when implementing algorithms that don't require result-dependent branching; the scalar rate is the key spec when it is necessary that branching depend on the result, e.g., in general-purpose computations.

Figure 3 is a block diagram of the ADSP-1220 Floating-Point ALU. Housed in a 144-pin grid-array package, it has two 32-bit input ports and one 32-bit output port. A pair of control inputs configure the device for either one- or two-port operation. Four input registers are available for each of the A and B operands; each input port can load any of the eight input registers. At the output, the 64-bit output register is multiplexed into the 32-bit output port.
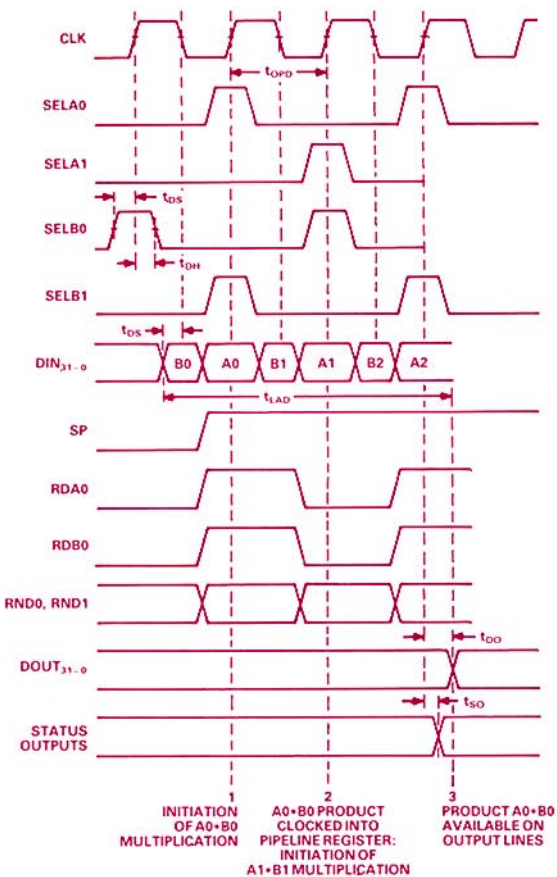

Figure 3. ADSP-3220 Floating-Point Arithmetic & Logic Unit (ALU).

In three-port operation, full 10-Mflops throughput is available for 64-bit double-precision operations; two 64-bit operands are loaded on each cycle, and internal operations are performed with 64-bit wide data paths. The ALU output is latched into a pipeline register, then formatted and latched into the output register. Figure 4 shows the ADSP-3220 timing for DP, two-input-port addition. ▶

Figure 2. ADSP-3210 Single-precision floating point multiply timing diagram (direct operand feed). MSWSEL is held high.
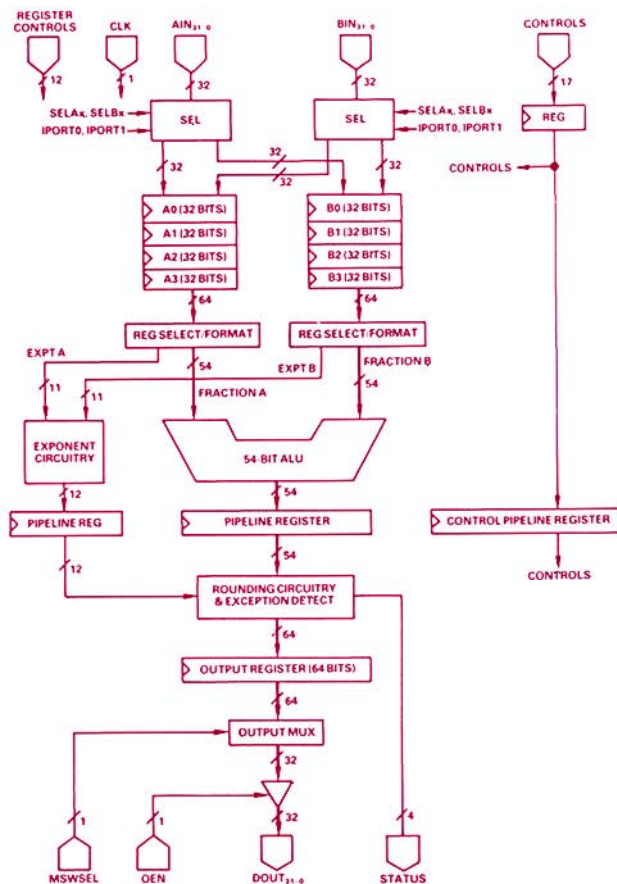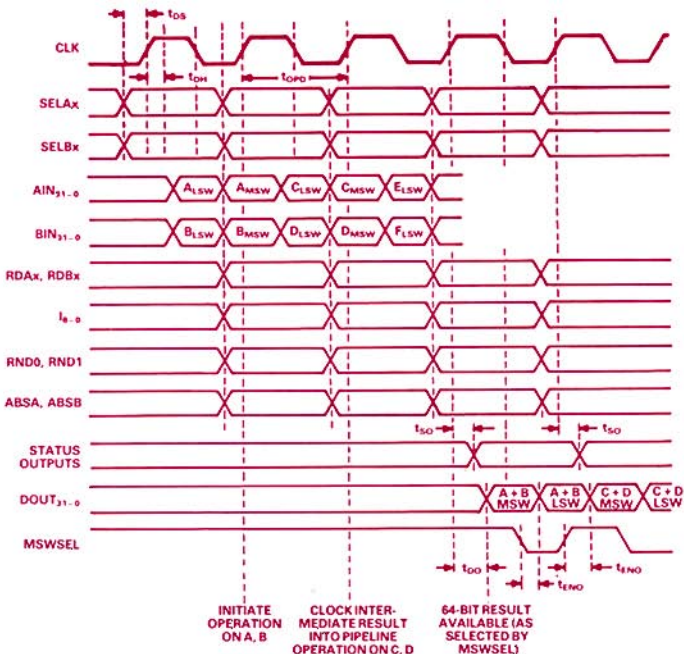

Figure 4. ALU timing for double-precision 64-bit, two-port addition (direct operand feed).

FAST, FLEXIBLE CMOS ICS SIMPLIFY DESIGN OF DSP SYSTEMS
Program Sequencer, Address Generator Combine High Thruput, Low Power Dissipation
ADSP-1401, ADSP-1410: Key Components of Word-Slice™ Microcoded Systems

by David Fair

The ADSP-1401* Program Sequencer and the ADSP-1410* Address Generator are members of a second-generation family of microcoded 16-bit building-block devices. They make possible high-performance, relatively compact fast arithmetic processors (i.e., number crunchers), using fixed- or floating-point multipliers and ALUs (arithmetic/logic units), to execute algorithms for digital filters, FFTs (fast Fourier transforms), and matrix operations in "real time."

MICROCODED SYSTEMS

A microcoded system employs building-block ICs to construct a high-speed processor (Figure 1). This gives the designer increased control over the system's architecture, with sufficient latitude to meet very high throughput specifications.
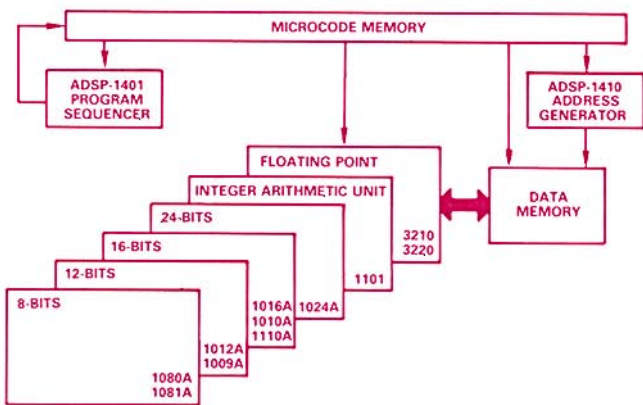

Figure 1. Typical microcoded DSP or numeric processing system.

The power of a microcoded system lies in the fact that, during each clock cycle, each component can execute an instruction; this parallel operation allows the system to attain high throughput. The operation of each component is governed by the system's microcode memory, which contains the microcode controls (0s and 1s). On a cycle-by-cycle basis, these controls are fed to each component, telling it what instruction to execute. The microcode memory's width is a function of the number and kind of components in the microcode system; its depth is proportional to the length of the overall microcode program, or microprogram.

Figure 2 is an example of bit disposition in a microcoded system. A set of instructions is stored in a wide (e.g., 27-bit) microcode memory. The memory word-width is apportioned so that—simultaneously—seven bits provide instructions to the ADSP-1401 Program Sequencer, ten bits instruct the ADSP-1410 Address Generator, two bits control chip-select and read-write for memory, one bit controls a latch at the data destination, and one bit controls output-enable for a buffer. The remaining instruction bits might control the mode of operation of a multiplier-accumulator, ALU, data converters, etc.

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*Use the reply card for technical data.
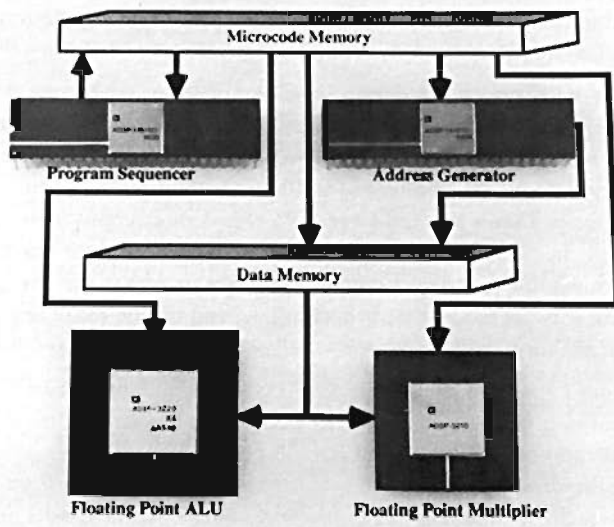
In the past, the sequencing and address-generation functions were pieced together with numerous power-hungry bit-slice devices, which tended to increase the system's cost and complexity. The second-generation ADSP-1401 and ADSP-1410 are called Word-Slice™ devices because they are flexible building blocks in which the modular address unit is the 16-bit word, rather than the space- and power-consuming 4-bit nybbles typical of some conventional "slice" architectures.

Typical alternatives to microcoded systems include complex hard-wired logic and single-chip digital signal microprocessors. Besides having software support, microcoded systems occupy less board space, dissipate less power, and are easier to design and modify than complex hard-wired logic arrays. Compared with single-chip DSPs, microcoded systems have greater flexibility and higher performance.
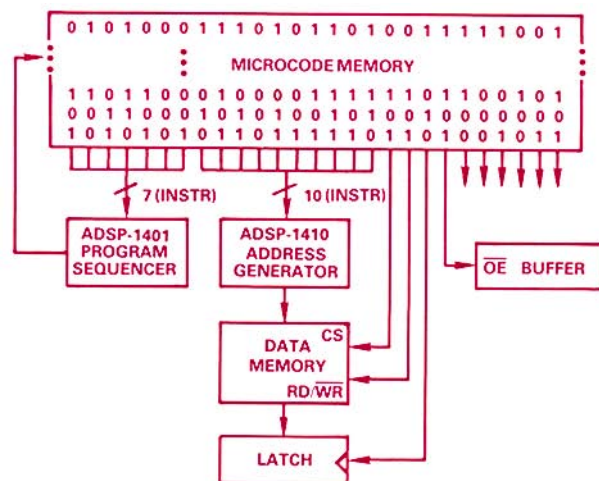

Figure 2. Disposition of simultaneous bits in microcode memory.

THE COMPONENTS

Program Sequencer The brain of a microcoded system is its program sequencer, which moves the system through the microcode memory. A representative sequencer is the ADSP-1401, shown in Figure 3, a high-speed, 16-bit microprogram controller optimized for numeric processing and digital signal processing (DSP). Such devices usually perform an elementary function: storing the current microcode address (instruction number) in the program counter, incrementing it, and outputting it. This activity corresponds to simply stepping through the instructions of a program.
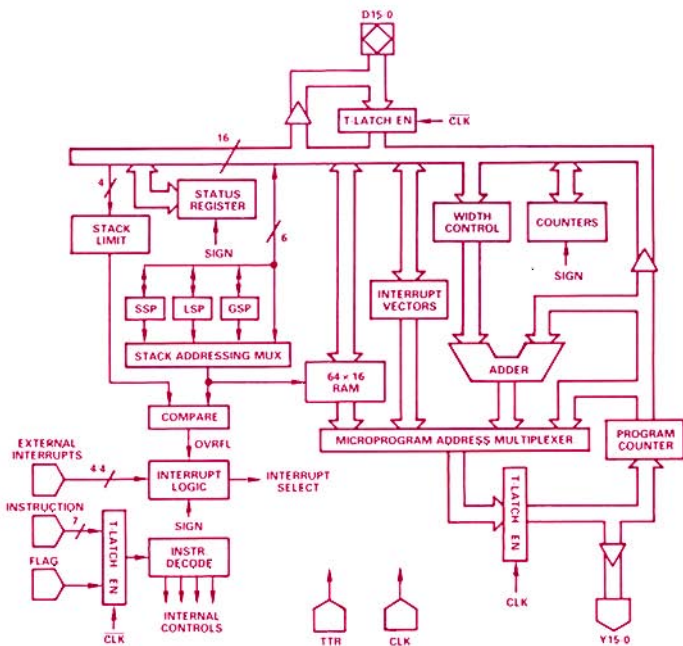

Figure 3. Functional block diagram of ADSP-1401 Data Address Generator.

However, limiting any computer to executing straightline code is unduly restrictive. For this reason, microprogram sequencers must also have the flexibility to handle subroutine jumps, branches, interrupts, and indirect jump addresses. For example, the ADSP-1401 monitors the conditions and instructions to determine the next microprogram memory address, which can come from: i) a simple increment of the current address, ii) an absolute or relative jump, iii) a jump address from the internal RAM, iv) a subroutine call or return, or v) an internal interrupt vector.

The ADSP-1401 has a number of features to make such operations fast and painless, starting with a Look-Ahead™ pipeline and 25-ns (max) clock-to-address delay:

Large addressing range (64K of program memory)
On-chip storage and control of ten prioritized and maskable interrupts
Four decrementing event counters
Absolute, relative, and indirect addressing capability
Download capability (writeable control store)
A dynamically configurable 64-K read-write memory for storing subroutine linkage, jump addresses, counters, pointers, and status register.

Address Generator For addressing requirements in digital signal processing, array processing, and high-performance computing, a microcoded system can splice together several 4-bit- or 8-bit arithmetic and logic units. More powerfully, and with a substantial re-

duction in board space, it can use devices such as the ADSP-1410 high-speed 16-bit general-purpose address generator (Figure 4).

This low-power CMOS device rapidly generates data-memory addresses required by routines such as digital filters, FFTs, matrix operations, and DMAs, in a single cycle; specifically, it

Outputs an address pointer to data memory;
Modifies the pointer by an offset value to determine the next memory read/write address;
Compares the output pointer to a preset value and, if equal, re-initializes the pointer with a value stored on-chip.

In addition to its high speed (23-ns clock-to-valid-address delay), the ADSP-1410 has two ports, a Look-Ahead pipeline, and 16-bit architecture, which includes a 16-bit ALU, digital comparator, and 30 16-bit registers. The registers are organized into four files: 16 address registers, 6 offset registers, 4 comparison registers, and 4 initialization registers. The ADSP-1410 includes a bit-reverse MUX, useful in FFT addressing.

One address generator is often adequate for an application. However, where the needs for high throughput require simultaneous 16-bit addressing for memory elements in a system (e.g., data memory and coefficient memory), more than one address generator may be used; also, if more addresses are needed than can be expressed by 16 bits, two ADSP-1410s can be cascaded for 30-bit addresses, with a minimal speed penalty. Alternatively, if time permits, a single ADSP-1410 can produce a 30-bit address in two cycles.

Available in both plastic and ceramic 48-pin dual in-line packages for the 0°C to 70°C and −55°C to +125°C temperature ranges, the CMOS ADSP-1401 and ADSP-1410 respectively dissipate only 375 and 350 milliwatts maximum. Prices (100s) start at $65. and $45. ▶
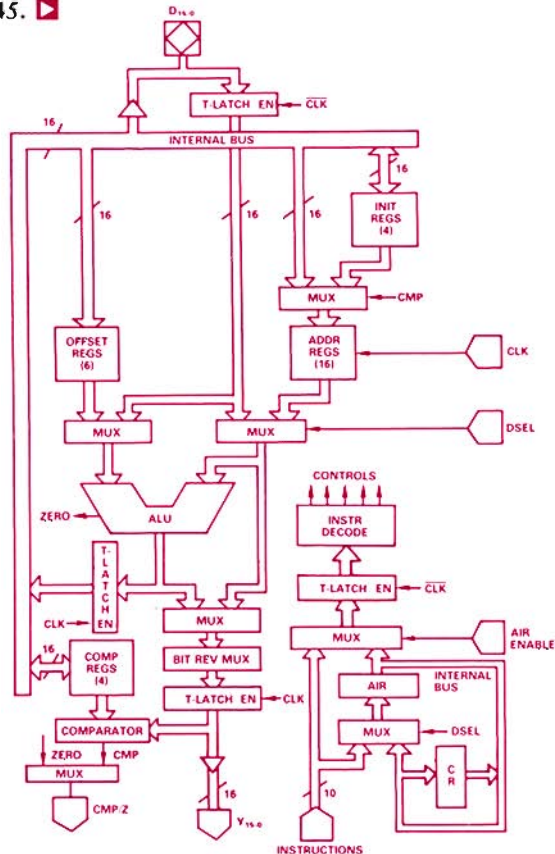

Figure 4. Functional block diagram of ADSP-1410 Microprogram Sequencer.

REAL-WORLD INTERFACE CARDS FOR IBM PERSONAL COMPUTERS

RTI-800 Family Provides Analog & Digital Inputs & Outputs for PC, PC/XT, PC/AT
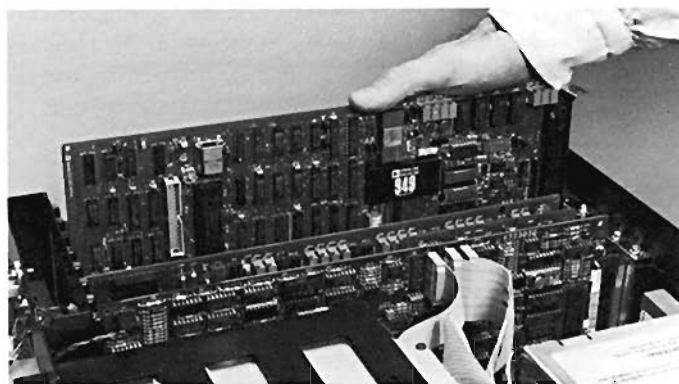## Hardware and Software-Compatible; Throughput to 71,000 Hz; 12-bit ADC & DACs

Four boards in the the RTI-800 series, the newest members of the RTI™ family of board interface products, provide fast, flexible and transparent input/output (I/O) interfacing between IBM (and IBM-compatible) personal computers and the real world of current, voltage, switch closures, and detectable events. Key features of these boards include high speed (up to 71 kHz throughputs) and channel density (e.g., up to 32 single-ended analog input channels), as well as software drivers for high-level languages, such as BASIC, Pascal, C, FORTRAN, and Turbo Pascal—running under MS-DOS.

The series consists of the RTI-800 and RTI-815 Multifunction Analog and Digital Boards,* the RTI-802 Analog Output Board,* and the RTI-817 Digital Input/Output Board.* Their input/output functions are summarized in the table:

	Analog Input Ch. (12-bit)	Analog Output (12-bit)	Digital Input Channels	Digital Output Channels	Counter-Timer Channels
RTI-800	16-32	–	8	8	3
RTI-815	16-32	2	8	8	3
RTI-802	–	4-8	–	–	–
RTI-817	–	–	(8 + 8 + 8: 24 total)		

Typical applications include electronic test, quality assurance, data logging, machine control, process control, robotics, imaging, analytical data acquisition, and instrumentation.

RTI-800 and RTI-815 Figure 1 shows the architecture of the RTI-800 and RTI-815; they differ only in that the RTI-815 has two analog output channels with 12-bit resolution, in addition to the RTI-800's functions. Both boards accept 8 (16 optional) fully differential analog inputs or 16 (32) single-ended or pseudo-differential (off-ground common terminal for all channels) analog inputs. The input signal is amplified by an instrumentation amplifier, with software programmable gain ranges of 1, 10, 100, and 500 V/V, permitting nearly three decades of decimal floating-point operation to be programmed. Data is converted by a 12-bit ADC chosen for 25-μs, 12-μs, or 8-μs conversion time, for system throughput rates of up to 71,000 samples per second.

In addition to the analog inputs (and outputs, RTI-815), both boards have two 8-bit digital ports for TTL-compatible inputs and outputs. For compatibility with solid-state relay subsystems, such as Opto 22, the digital output polarity is inverted (active low); the output can sink up to 8 mA. Also available are 3 counter/timer channels, for *event counting* (to 65,531 at up to 100-kHz rate), *frequency measurement* (to 100 kHz with programmable gate time from 1μs to 655.35s and 16-bit resolution), *pulse outputs* (programmable widths from 2μs to 655.35 and 16-bit resolution), and *time-proportional outputs* (programmable periods from 1μs to 655.35 s with 0 to 100% duty cycle), with timing error of 0.01%.

Available optionally with screw terminals for field wiring, each RTI-800/815 card occupies one long slot in the IBM expansion bus, and 16 consecutive bytes in a switch-selectable 512-byte block. Several modes of operation are possible, since hardware is present to support direct memory access (DMA), polled status, or interrupt operation. Software includes calibration routines and callable machine-language routines for analog and digital I/O.

RTI-802 The RTI-802, occupying a long slot in the PC—and four consecutive bytes in memory, contains four or eight d/a converters, which produce constant voltage proportional to the applied digital codes. These outputs have many uses, including control-valve positioning, test stimuli, and set points in control systems.

RTI-817 The RTI-817, which can fit in a short slot and occupies 4 consecutive bytes in memory, has 24 input or output lines, collected into three independently selectable 8-bit ports, compatible with 16- and 24-position solid-state-relay subsystems. It can generate Interrupts on change-of state.

All boards in the RTI-800 series are powered from the PC's +5-volt supply. The analog boards, RTI-800 and RTI-815 (5.5 watts), and RTI-802 (2.5 watts) have on-board dc-to-dc converters to provide all necessary operating voltages. ◗
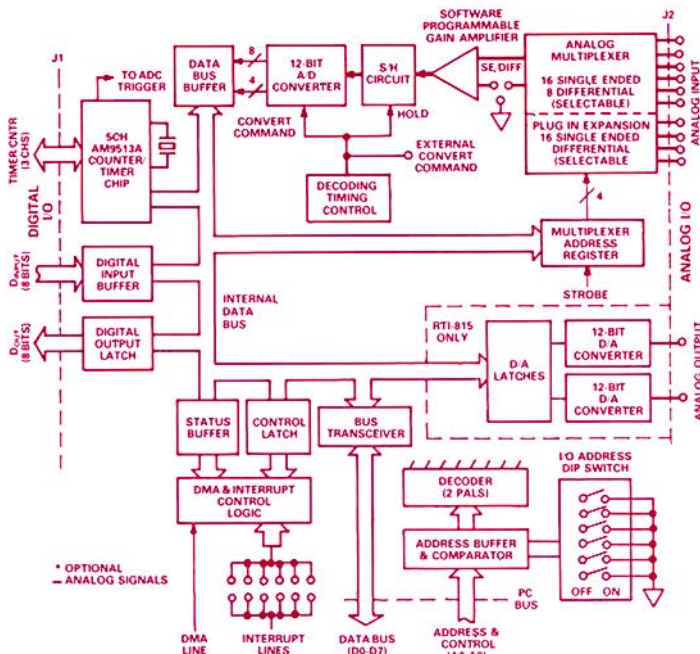

Figure 1. Block diagram of the RTI-815 and RTI-800.

RTI™ is a trademark of Analog Devices, Inc.

*Use the reply card for technical data.

μP-BASED AUTORANGING THERMOCOUPLE METERS
AD2070 & AD2071 Offer High Accuracy, Autoranging, Communication Options
Wide Choice of Thermocouples: J, K, T, E, R, S, C, B, J DIN, T DIN

With the AD2070 and AD2071* high-performance 4½-digit microprocessor-based autoranging single-channel thermocouple meters, temperatures from −328°F to +4,200°F (−200°C to +2,315°C) can be measured accurately with a wide variety of thermocouples: J, K, T, E, R, S, C, B, J DIN, or T DIN.† The AD2070 is programmed at the factory to work optimally with one of these thermocouple types, as specified by the user; the AD2071 is a universal meter that the user can switch-program to work with *any* of these thermocouples.

The meters combine autoranging, e.g., +1989.9°F, +2023°F (K-type), automatic gain and offset correction, cold-junction compensation, thermocouple linearization, and scaling in either °C or °F—as chosen by a switch setting—all under microprocessor control. In addition, their communication options simplify temperature recording with computers, strip-chart recorders, or printers.

The AD2070 and AD2071 can be used wherever thermocouples are employed and accurate temperature measurement and readout are required. Possible uses abound in laboratories and industrial process monitoring and control, test equipment, and quality control.

Temperature is displayed on large 0.56"-high (14.3mm) LEDs, and temperature output is available digitally in 7-bit standard ASCII character-serial format. Optional isolated RS-232 or 20-mA serial outputs are available for easy interface to printers and other data-logging peripherals. An isolated and linearized *analog* output (1 mV/°C or °F) is also available for driving recorders and analog instruments, or as a signal input for analog-input control systems.

Depending on thermocouple type and range, the meters have resolutions of 0.1° or 1° (C or F). For such popular thermocouple types

as J, J DIN, K, T, T DIN, and E, resolutions are 0.1°C or °F (except for 2000°F to 2282°F, Type K); and accuracies are to within 0.8°F or 0.4°C (± ½ LSD), including conformity errors, cold-junction compensation errors, and gain-and-offset errors.

Both meters are available with four isolated ports (input, power, digital output, and analog output). Isolation specifications include: 1,400-volt peak common-mode between the input and power-line ground, 300-volt peak thermocouple short to the ac line, and 500 volts peak for the analog and digital outputs to power and input sections.

Overrange indication, overvoltage protection, and open-thermocouple detection are provided. For improved reliability, each meter is burned-in for 168 hours at 50°C, with on/off power cycles (the operating temperature range is −10°C to +50°C).

The AD2070 and AD2071 are supplied in a heavy-gauge, rugged metal case dimensioned according to DIN/NEMA standards. Three power options are available: 120V ac, 240V ac, and +7.5 to +28V dc. Prices of single units are $399 (AD2070) and $439 (AD2071). ▶
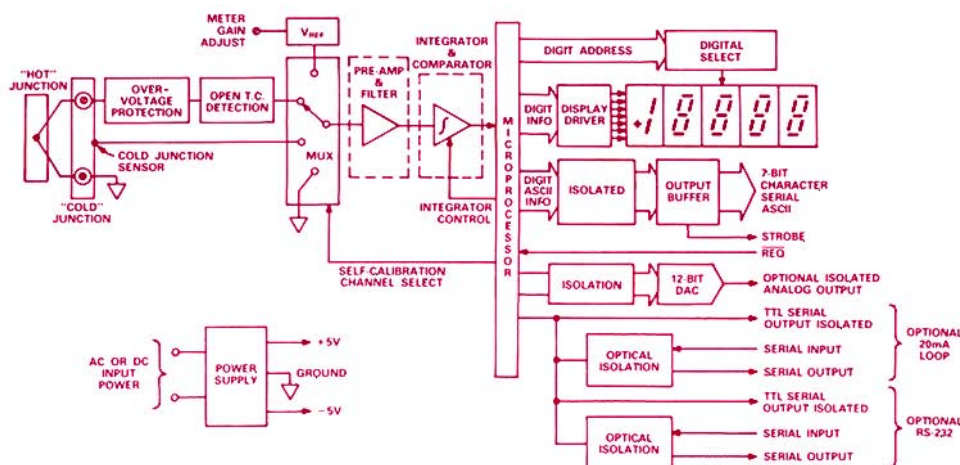

Figure 1. Functional block diagram of the AD2070/2071.

*Use the reply card for technical data.

†Thermocouples come in many forms, depending upon the choice of dissimilar metals used, the temperature range, and the requirements of the application. Because any two dissimilar metals that are in contact can form a thermocouple, standards for composition have been established and calibration tables for output voltage vs. temperature published (e.g., by the National Bureau of Standards, in the U.S., and *Deutsche Industrie Normenausschuss* (DIN) in Germany).

Among the most popular types are Type J (iron-Constantan, for reducing atmospheres—temperatures to 760°C; typical sensitivities 50-60 μV/°C), Type K (Chromel-Alumel, for clean oxidizing atmospheres—temperatures to 1350°C; typical sensitivities 1-50μV/°C), and Type T (copper-Constantan, for mildly oxidizing and reducing atmospheres where moisture is present—temperatures to 400°C; typical sensitivities 40-60μV/°C).

3 NEW 4-DAC DIPS: 8-AND 12-BIT QUAD D/A CONVERTERS

Monolithic AD7225: Four 8-Bit DACs, Double-Buffered, Separate Reference Inputs
12-Bit Hybrid AD394: Four 4-Quadrant Multiplying DACs; AD395: Four Two-Quadrant M-DACs

by Bill Gotschewski and Paschal Minogue

The world's first families of self-contained quad DACs, four voltage-output DACs in an IC package, originated with the 4×12-bit AD390,* in 1982 (*Analog Dialogue* 16-3), and the 4×8-bit monolithic AD7226,* in 1983 (17-2). A quad DAC basically consists of 4 addressable d/a converters with independent voltage outputs on a silicon chip or hybrid substrate; in these early models, all DACs shared a common reference.

Now three new quad DACs add features that extend the range of applications. The 12-bit AD394 and AD395* consist of 4 CMOS multiplying DACs and output amplifiers, differing only in their output-amplifier architecture: the AD394 contains four 4-quadrant 12-bit CMOS multiplying DACs, in which each bipolar analog input is multiplied by an offset-binary digital code, while the AD395—a quad of 2-quadrant multiplying DACs—multiplies each bipolar analog input by a unipolar digital code. The LC²MOS (linear-compatible CMOS) AD7225* is a monolithic quad of 8-bit DACs, in a narrow (0.3") 24-pin plastic or hermetic (cerdip or ceramic) DIP, with double-buffered binary inputs and independent fixed or variable positive voltage-reference inputs.

The table summarizes similarities and differences among today's quad DACs:

CHARACTERISTIC	AD390	AD394	AD395	AD7225	AD7226
No. of DACs	4	4	4	4	4
Resolution, bits	12	12	12	8	8
Independent Refs?	NO	YES	YES	YES	NO
On-Board Ref?	+10 V^A	NO	NO	NO	NO
Reference Range	+5 to +11V	±11V	±11V	2V to (V_DD −4V)	
Mult. Quadrants	1; 2 optional	4	2	1^B	1^B
Ranks of Latches	2	1	1	2	1
Coded addressing?	NO	NO	NO	YES	YES
Simultaneous update?	YES	YES (common)	YES (common)	YES	NO
Construction	Hyb.Bip.	Hyb.CMOS	Hyb.CMOS	Mono.CMOS	Mono.CMOS
Package	28-pin her. ceramic double-DIP	28-pin her. metal double-DIP	28-pin her. metal double-DIP	24-pin plas/her.^C 0.3" DIP	20-pin plas/her.^C 0.3" DIP

^A External reference may be used. 2.5 mA are available for external loads.
^B One-quadrant devices can be operated in two quadrants with simple external circuitry.
^C Cerdip or ceramic.

Why Quad DACs? Multiple d/a converters save board space, time, and money. They are useful in systems, instruments, or apparatus where multiple analog phenomena are controlled from a common digital bus. Examples include automatic test equipment, state-variable filters and oscillators, multichannel precision gain controls, and flight simulators or other systems that involve multi-axis positioning or displays.

Multiple DACs make feasible the implementation of circuit structures, such as transversal filters, for parallel operation in real time without requiring digital multipliers and multiplier/accumulators.

AD7225 The AD7225 quad 8-bit DAC (Figure 1) has a separate reference input for each DAC channel and a double-buffered digital interface; it fits into a 0.3"-wide plastic or hermetic DIP. The DACs are connected in the voltage mode and each is buffered by a non-inverting on-chip follower-connected op amp capable of developing +10 volts across a 2,000-ohm load; benefits of this connection include high speed, low dynamic errors, and capability of single-supply operation.
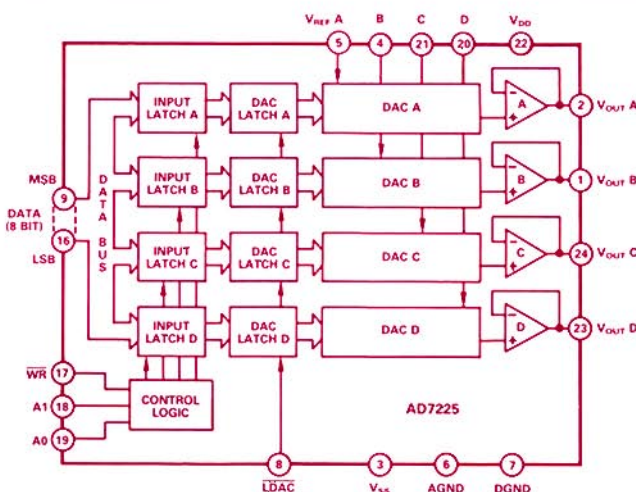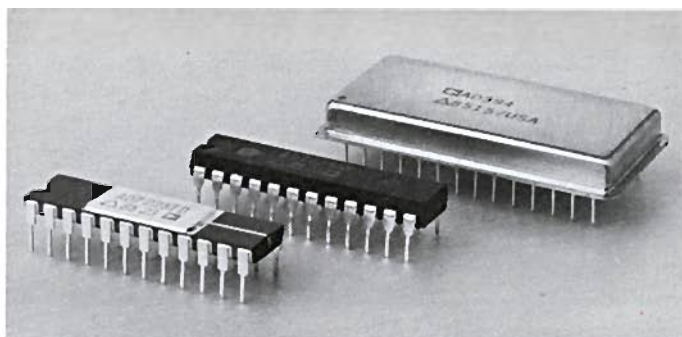
*Use the reply card for technical data.

Figure 1. Block diagram of AD7225 8-bit quad DAC.

Data arrives on a common 8-bit data bus and can be latched in two stages. This makes it possible to load each latch separately, then update the outputs of all four DACs simultaneously. The active-low controls are a $\overline{WR}$ (write) line, $\overline{LDAC}$ (load DAC) line; two internally decoded address lines, A0 and A1, choose one of the four input latches to be loaded.

The analog input has a range of $+2$ volts minimum to $(V_{DD} - 4)$ volts, e.g., 11 volts with 15-volt supplies. For conventional DAC applications, either a fixed or variable reference may be used. The DAC may also be used to provide digitally controlled attenuation for a positively biased ac signal. One of the on-chip DACs may itself be used to generate a digitally controlled reference voltage for other DACs on the same or other chips—or for the system.

The AD7225 is characterized for operation with single or dual supplies with no user trims required. Single-supply operation is specified from $+14.25$ V to $+15.75$ V, with a $+10$-volt reference. Operation with dual supplies will give faster settling time (5 μs vs. 7 μs); dual operation calls for positive power supply voltage from $+11.4$ V to $+16.5$ V and negative supply voltage from -4.5 V to -5.5 V, with input reference signals from $+2$ V to $(V_{DD} - 4$V$)$.

Three sets of temperature grades are available: devices with KN and LN suffixes, specified for 0°C to $+70$°C, are packaged in plastic; BQ and CQ grades, specified for -25°C to $+85$°C, and

TQ & UQ, for −55°C to +125°C, are hermetically packaged in cerdip or ceramic. All grades of the AD7225 specify ±1 LSB maximum differential nonlinearity; total maximum error without external adjustments is ±1 LSB for LN/CQ/UQ grades, ±2 LSB for KN/BQ/TQ grades. Prices start at $18.50 (100s) for AD7225KN.

AD394 and AD395 These devices (Figure 2) contain four CMOS 12-bit d/a converters and output amplifiers, respectively connected for 4- or 2-quadrant multiplication, with only 750-milliwatt maximum dissipation. The AD394 multiplies a positive or negative digital number by a positive or negative analog voltage, for a ±10-volt bipolar output range, with correct polarity relationships, while the AD395 multiplies a positive digital number by a positive or negative analog voltage, with an output sign inversion (i.e., $V_{OUT} = -D\,V_{REF}$, where D is the magnitude of the digital number and V_{REF} is the positive or negative analog input voltage).
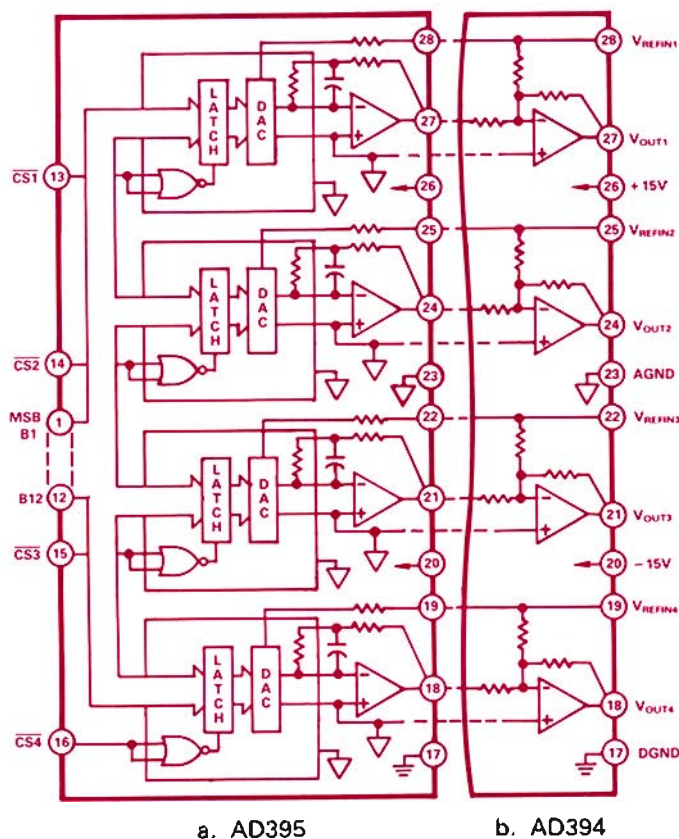

Figure 2. Block diagrams of quad 12-bit DACs. a. Functional block diagram of two-quadrant multiplying DACs. b. AD394 four-quadrant multiplying-DAC architecture.

The 12-bit parallel digital input of these devices interfaces easily to most 12- and 16-bit bus systems. Each internal 12-bit CMOS DAC chip includes an independently addressable register, allowing DACs to be loaded separately or in any combination. Operating with ±15-volt supplies, the converters guarantee monotonic behavior over the specified operating temperature range and a maximum settling time of 15 μs to ±½ LSB. Laser trimming insures that maximum nonlinearity is less than ±½ LSB for KM and TM grades, and less than ±3/4 LSB for JM and SM grades.

Housed in metal packages, the AD394/395 are available in two sets of operating temperature grades—JM/KM for 0°C to +70°C, and SM/TM for −55°C to +125°C. MIL-STD-883C versions of the S and T grades are available. Prices (J, 100s) start at $115.

APPLICATIONS

As noted above, these multiple DACs are useful to the designer whenever the design calls for a number of 8- or 12-bit DACs or digitally programmable analog gain controls (especially if they must track), where cost and space must be conserved. Some natural areas for application are mentioned above.

An interesting applications area (one which may be suggestive of other creative applications for these devices) lies in the design of programmable hybrid (analog-digital) transversal filters for analog signals. Their principal advantage is that the required multiplications are performed simultaneously in real time in the analog domain, greatly simplifying software and employing low-cost multiplying DACs rather than quantities of somewhat-more-expensive digital multipliers. This application is described in somewhat greater detail in the AD7225 data sheet. If 8 bits aren't enough, members of the AD390 family can be used in similar fashion.

A finite-impulse-response (FIR) transversal filter is a tapped delay line for which the signals at the tap points, x(n − i), are individually multiplied by coefficients, h_i, and the results summed to produce the output (see inset to Figure 3):[1]

$$y(n) = \sum_{i=0}^{N-1} h_i\, x(n-i) \tag{1}$$

The coefficients may be obtained directly from the desired time-domain impulse response, if known, for a given sampling rate; otherwise, they may be calculated from the desired frequency response, using the Remez exchange algorithm.

Figure 3 shows a flexible implementation of a filter having three delay stages (4 taps). The coefficients are set digitally, using an AD7226 quad DAC to multiply the reference voltage by the individual coefficient values. The AD7224 DAC* sets the reference, hence the overall gain, digitally.
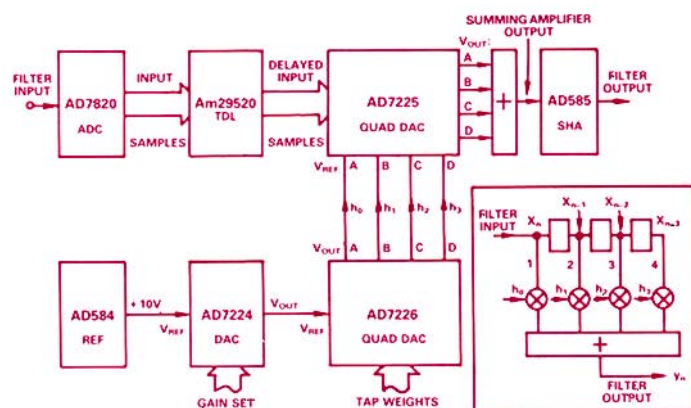

Figure 3. Programmable analog/digital transversal filter application. Block diagram of system employing quad DACs for 3-stage filter. Inset: general block diagram of transversal filter.

The input signal, after passing through an anti-aliasing filter, is converted to digital in the AD7820*, then processed by a delay line (the Am29520 here). The delayed outputs are latched simultaneously into the AD7225's DACs, where they are multiplied by the coefficients; and the results are summed (by an analog summing amplifier), deglitched and held constant by a sample-hold (while the DACs are updated), and smoothed by an output filter. ▶

[1]See Chapters 6 and 21 in *Analog-Digital Conversion Handbook*, Third Edition, Daniel H. Sheingold, ed. Englewood Cliffs NJ: Prentice-Hall, 1986.

SOFTWARE-PROGRAMMABLE 12-BIT DATA-ACQUISITION SYSTEM
AD369 Has 50-kHz Throughput Rate, Is Complete in a Standard 28-Pin Package
No Missing Codes Over Temperature

by Ed Garibian

The AD369* is a complete hybrid 12-bit single-channel data-acquisition system (DAS) for system designers with cost-, space-, and time constraints. It combines (Figure 1) a software-controlled programmable-gain instrumentation amplifier (PGIA), a track-and-hold amplifier (T/H), and a 12-bit a/d converter, all housed in a double-width 28-pin hermetically sealed metal package. System throughput is 50 kHz for programmed gains of 1, 10, and 100—and 20 kHz at a gain of 500.
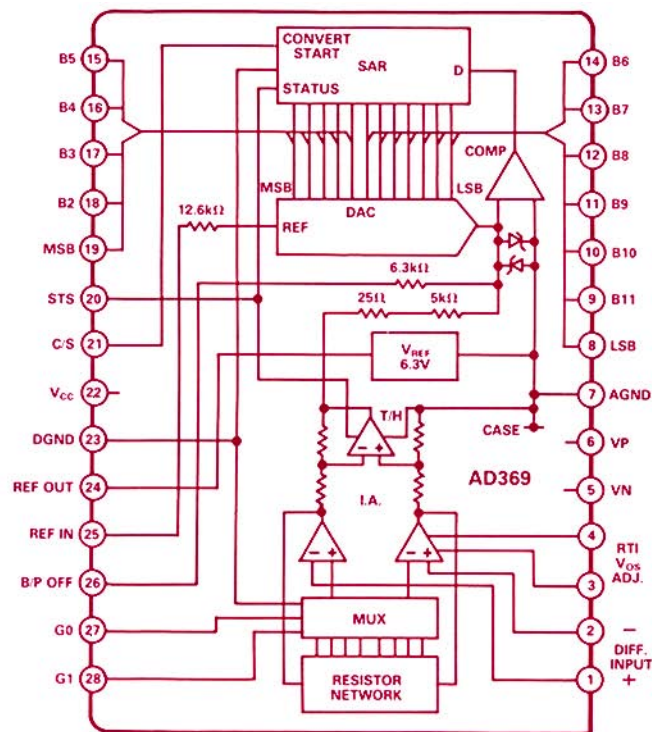

Figure 1. Functional block diagram of the AD369 with pin designations.

Maximum conversion time of the AD369's successive-approximation ADC is 15 μs; acquisition time of the T/H (with internal hold capacitor) is 3 μs, maximum. These numbers, compatible with the short settling time of the front end (Figure 2), combine to give the AD369 a pipelined system throughput rate of better than 50 kHz at gains of 1, 10, and 100. The DAS is available in two grades; both guarantee no-missing-codes over the industrial temperature range of −25°C to +85°C. The AD369BM has a guaranteed maximum integral nonlinearity (INL) of ½LSB; INL for the "A" grade is guaranteed to be a maximum of ¾LSB.

The software-programmable-gain amplifier allows the user to choose full-scale input ranges of 10, 1, or 0.1 volts, and 20 millivolts. With the 12-bit resolution of the ADC, signals of 5 microvolts can be resolved in the G = 500 mode; this is a dynamic range of 126 dB, i.e., $20 \log_{10} (500 \times 4,096)$. The precision differential input of the AD369 provides excellent common-mode rejection
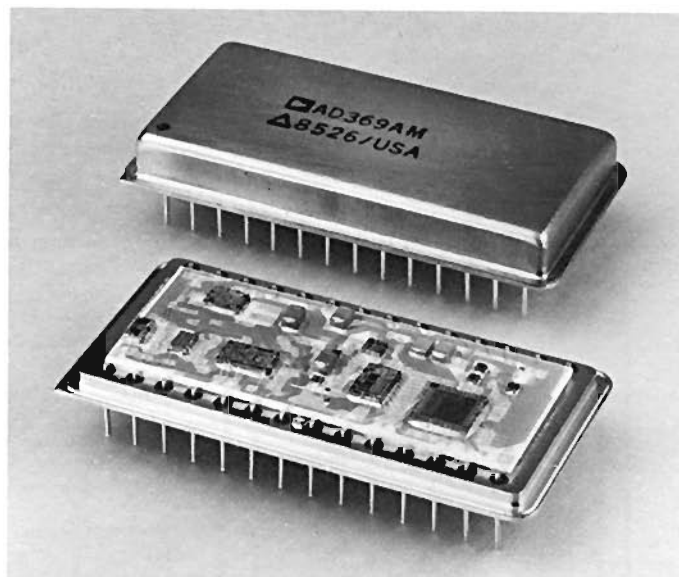
capability (108 dB min, with G = 500) and can be used with bipolar or unipolar input sources.

Typical applications include automatic test equipment, wide dynamic-range measurement systems, analytical and medical instrumentation, multi-channel systems with mixed high- and low-level signals (with the addition of an external multiplexer), and other systems that require a small, complete sampling a/d converter with differential input and programmable gain. Devices of this kind should be of especial interest to manufacturers of general-purpose data-acquisition systems and instrumentation, as well as board-level DAS products for personal-computer interfacing.

The AD369 provides a completely specified and tested combination of all the critical functions of a data-acquisition system in a space-saving 28-pin metal package. Typical power consumption for this complete DAS is 775 mW. Prices in 100s are $107/$124 (AM/BM). ▶
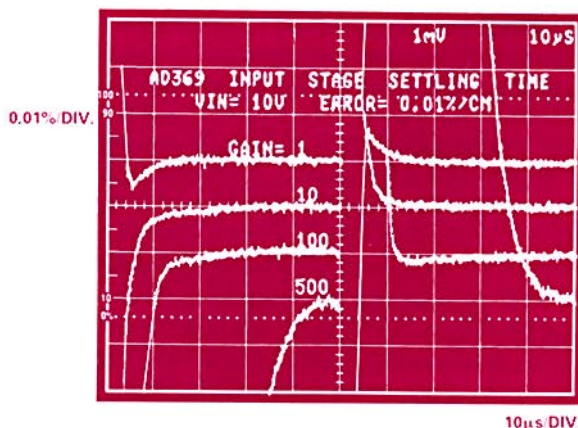
Figure 2. Settling time of the input stage for a 10-volt step. Each horizontal division is 10 μs and each vertical division is 0.01% (i.e., less than 1LSB).

ULTRAFAST HIGH-RESOLUTION SAMPLING A/D CONVERTERS
CAV-1220: A 12-Bit Converter with 20-MHz Sample Rate
CAV-1040: 40 Million 10-Bit Conversions per Second

by Don Brockman

Models CAV-1220* and CAV-1040* are ECL-compatible video-speed sampling a/d converters built on 7″ × 5″ (177.8 × 127mm) cards. The CAV-1220 has 12-bit resolution and a maximum data rate of 20MHz; and the CAV-1040 has 10-bit resolution with a 40-MHz max sample rate. Both devices are complete and self-contained, with track-and-hold circuitry and all necessary timing.
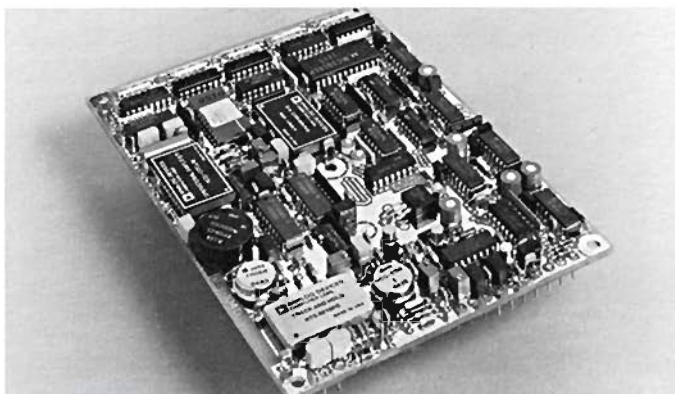
The newest additions to the Analog Devices family of card-level high-speed a/d converters, they are physically and electrically compatible with their lower-performance predecessors. For example, the CAV-1040 can replace the MOD-1020 in 10-bit circuitry, for a doubling of conversion rate in applications originally designed around the CAV-1020. Similarly, for 12 bits, the CAV-1220 can replace the CAV-1210—again providing a doubling of speed.

In radar applications, the CAV-1220's high word rates enhance ranging resolution, thus increasing system effectiveness, while the 12-bit signal resolution provides more fine structure than do lower-resolution converters. In imaging applications, the high speed and resolution improve overall system performance by increasing the contrast and/or color resolution. Other applications (for both) include communications, digital oscilloscopes, digital x-rays and other medical uses, TV studio digitizing, and real-time spectral analysis. Operating temperature range is 0°C to +70°C.

DIGITALLY CORRECTED SUBRANGING

Both converters achieve their combination of speed and resolution through digitally corrected subranging, a technique perfected at Analog Devices and employed for the rest of the CAV family, as well as CAV's predecessor, the MOD family. The technique consists of performing two "flash" conversions—the first obtains the m more-significant bits, the second obtains n + 1 less-significant bits—they are combined to form a "seamless" (m + n)-bit word.

Consider the CAV-1220, for example (Figure 1): while the input signal is frozen in a track-and-hold, a 5-bit flash encoder performs a coarse conversion, the results of which are stored in a register. The results are converted back to analog in a 5-bit-resolution, 12-bit-accuracy very-high-speed DAC, and compared with the de-

layed output of the track-and-hold, giving a difference—or residue—which is amplified to provide a signal that is referenced to full range for an 8-bit flash encoder. The output of the 8-bit encoder thus provides a digital output representing the input's fine structure; it is combined with the output of the 5-bit encoder in a manner that provides a 12-bit output word with arithmetic cancellation of errors that are due to the limited resolution and accuracy of the 5-bit encoder.

The internal timing of the converters is *pipelined*. This means that conversions can be performed at a 20-MHz rate, even though the conversion time is 155ns plus 1 clock period (50ns at 20MHz) for the CAV-1220, and 100ns plus 1 clock period (25ns at 40MHz) for the CAV-1040. An analog delay line, which provides for the output of the track-and-hold to reach the difference amplifier at about the same time as the analog value from the DAC, makes it possible to acquire a new input value for the next conversion while the earlier conversion is completed.

PERFORMANCE

CAV-1220 Full-scale analog input range is ±1.024V, into 1,000 ohms. Total error at dc, including nonlinearity, is 0.0125% of full scale. Maximum nonlinearity vs. temperature is specified at 15 ppm/°C, with maximum gain drift of 150 ppm/°C. Initial offset voltage is adjusted to zero with an on-card potentiometer. RMS signal-to-noise ratio is specified at 65dB, minimum, with a 540-kHz analog input. Other specifications include maximum aperture jitter of 25ps (rms), 100-ns transient-response time, and 200-ns overvoltage recovery time. Typical small- and large-signal 3-dB analog bandwidths are 40MHz and 35MHz.

CAV-1040 For use in digital communications, minimum signal-to-noise and noise-power ratios are 56 dB and 47 dB. For radar and spectrum analysis, ac linearity is specified in terms of spurious in-band signals generated at various input signal frequencies at a 40-MHz encode rate. Spurious signals from dc to 500kHz are at least 65dB below full scale, those from 500kHz to 2.3MHz at least −55dB, and from 2.3MHz to 10MHz, −48dB. Required power supplies (both devices) are ±15V, +5V and −5.2V. The standard model has small- (large-) signal analog bandwidths of 30 (20)MHz, while an "A" version has 60- (40)-MHz bandwidth. Prices (1's) start at $4,078 (CAV-1220 and CAV-1040). ▶
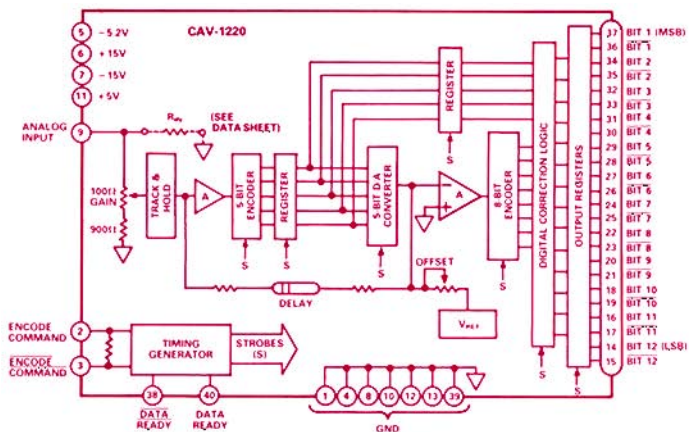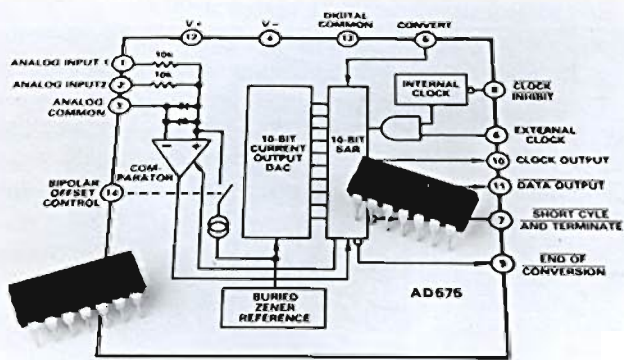

Figure 1. Block diagram of CAV-1220.

*Use the reply card for technical data.

COMPLETE MONOLITHIC SERIAL-OUTPUT 10-BIT A/D CONVERTER

AD575 Is Low-Cost and Compact: Housed In 0.3″ 14-Pin Plastic or Ceramic DIP
Has Flexible Timing, Converts in 30μs - No Missing Codes over Temperature

The AD575* is a complete 10-bit successive-approximation analog-to-digital converter on a single monolithic chip; it consists of a d/a converter, voltage reference, clock, comparator, successive-approximation register (SAR), and serial interface. No additional components are required to perform a full-accuracy 10-bit conversion in 30 microseconds.

Advantages of serial conversion include: fewer pin connections (the AD575 has 14), hence smaller packages (0.3″) and lower device cost; just one external data line (plus a clock line), hence lower system cost, easier isolation, and higher reliability; direct compatibility with serial processes; and faster availability of the most-significant portion of the data word. This last advantage is somewhat subtle: in circumstances where rough indication of the trend of the data is required in a hurry (e.g., polarity and gross magnitude), the AD575 can be short-cycled to 2, 4, 6, or 8 bits; at 2 bits, the data is passed within three clock cycles, and the converter is ready for the next request.

Why 10-bit conversion? Generally, 8 bits are too few, with resolution of 0.4% and log dynamic range of 48 dB—and often 12 bits are more than enough and too expensive besides. But an honest 10 bits constitutes a happy medium for many applications, with 0.1% resolution, 0.05% relative accuracy (K version), 60-dB dynamic range, and low cost.

The size, speed, and resolution of the AD575 make it an attractive choice for modems, disk drives, and remote or isolated data-acquisition systems, as well as for military and avionics applications. The AD575's short-cycle and timing features make it very easy to use, even with specialized processors such as the OKI MSM5218 speech compression/expansion chip.

OPERATION

The AD575 responds to four control inputs: CONV (convert), $\overline{\text{CLI}}$ (clock inhibit), XCL (external clock), and $\overline{\text{SCAT}}$ (short cycle and terminate); three outputs are provided: $\overline{\text{DO}}$ (data out), CO (clock out), and $\overline{\text{EOC}}$ (end of conversion, or "busy").

In response to a Convert command, the AD575 places on the clock output line a string of 11 pulses, and on the data-output line a se-

*Use the reply card for technical data.

quence of negative-true TTL levels ($\overline{1}$, $\overline{0}$), corresponding to the state of each bit. These levels, in synchronism with the clock, are guaranteed valid on the falling clock edge (starting with the MSB during the second clock cycle).

The status of the conversion is indicated by the end-of-conversion, or "busy," line, which goes high at the start of conversion and drops low at the beginning of the last clock cycle, to indicate that the SAR is ready to process a new conversion. Either the device's internal clock or an external clock, with frequency up to 450kHz, may be used. Figure 1 illustrates the timing when an external clock is used.
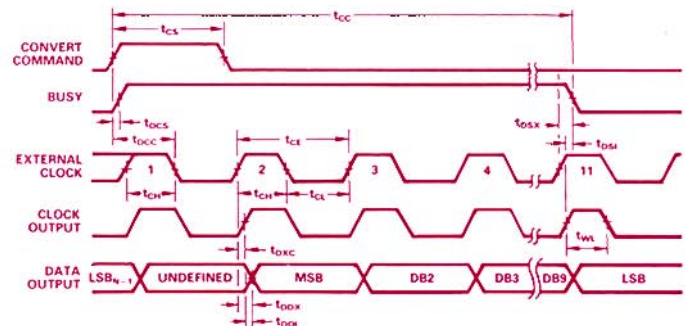

Figure 1. AD575 timing for externally initiated conversions.

The serial feature is useful in converting and communicating data to microprocessors with serial ports. Figure 2 shows an application with the 8085 microprocessor, in which the convert command, external clock, and AD575 data output are galvanically isolated via optocouplers.

The AD575 handles single-polarity or bipolar input signals (offset binary coding). It is available in three grades, J, K (0° to +70°C) and S (−55°C to +125°C). Over temperature, maximum relative accuracy error for the three grades is ±1/0.5/1 LSB, with no-missing-codes guaranteed. Prices (100s) start at $12.75. ▶
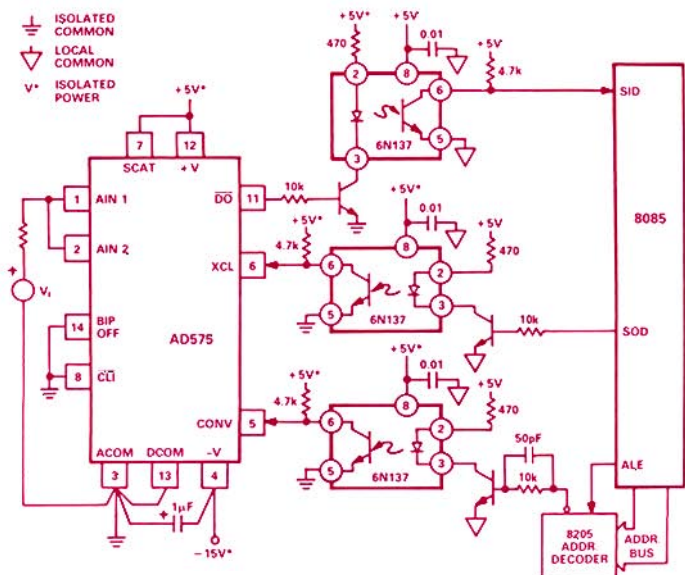

Figure 2. Interfacing the AD575 to an 8085 microprocessor via an isolated interface.

MONOLITHIC TRIPLE 4-BIT D/A CONVERTER
AD9702 Can Update Raster-Scan RGB Color Displays at 125 MHz or More (ECL)
## Versatile Logic Compatibility: Will Operate with Either ECL or TTL

The AD9702* is a monolithic integrated circuit containing three separate 4-bit digital-to-analog converters for red-green-blue (RGB) color-graphics display systems. It is housed in a 24-pin ceramic DIP (AD9702BW), with optional hermetic sealing (AD9702BD). The single-chip construction offers reduced cost and improved reliability over earlier three-chip designs. Price (100s) is $45 ($48 in hermetically sealed package).

Each d/a converter provides 16 gray-scale levels, for a total combination of 4,096 colors in red-green-blue displays. The AD9702's top update rate of 125 MHz (min) permits 4,096 different colors to be displayed on a 1,280-by-1,024-pixel, 60-Hz non-interlaced display.

Typical uses are in raster-scan displays, color graphics systems, and general video reconstruction applications, where it is important to have higher speed, plus smaller size, power, and price, than are available with hybrids.

The AD9702 is a complete single-chip raster-scan display subsystem. In addition to the three high-speed 4-bit d/a converters, it has all standard video control signals, including reference white, green sync, and composite blanking. The device is compatible with RS-170 and RS-343 standards. Three 4-bit input registers permit simultaneous updating of the d/a converters and reduce time skew to hold down the magnitude of glitches at the converter outputs. Glitches are spikes caused during code change when the time required for bits switching *on* differs from the time required for bits switching *off*; they are manifested principally at major transitions, such as 0111 to 1000[1].
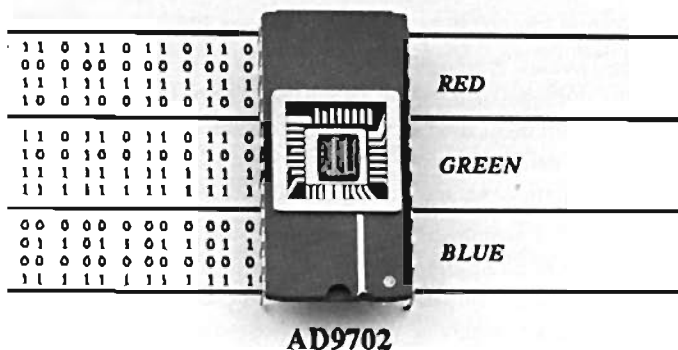
AD9702

The digital inputs are applied through TTL/ECL converters to registers within the AD9702. The switching of the inputs through the registers is controlled by the Strobe, Green Sync, Reference White, and Composite Blanking signals.

The high speed and small glitch of the AD9702 are attributable to its internal emitter-coupled logic (ECL) circuitry; in addition, for flexibility, a unique TTL/ECL interface allows the designer a choice of logic compatibility for all inputs; this can be accomplished by applying to the V_{CC} pin either +5V for TTL or ground for ECL logic levels.

For highest speed, ECL—using negative-true logic—gives a minimum top update rate of 125 MHz and requires a −5.2-volt supply. With TTL circuitry—employing positive-true logic—the minimum top update rate is 75 MHz, and both +5-volt and −5.2-volt supplies are normally called for (if necessary, the device can be connected for single-supply TTL operation).

The controls operate in this way: In normal operation, with Reference White, Composite Blanking, and Green Sync at digital "1", the analog output of each converter is in the gray-scale range, with intensity determined by its applied 4-bit code. When Reference White goes to "0", all analog outputs rise to zero voltage or current output, corresponding to reference white, or full-scale intensity. When Composite Blanking goes to "0", during the sweep retrace interval, all outputs are brought to −17.4 mA or −653 mV, a voltage level below the gray-scale range (i.e., "blacker than reference black"). When Green Sync goes to "0", the green analog output (only) will be −25 mA, or −938 mV, superimposing an analog synchronizing pulse for the CRT circuitry on the green intensity waveform.

The AD9702 is guaranteed to be monotonic over temperature. Key specifications include ±0.8% FS maximum nonlinearity, ±0.8% FS maximum differential nonlinearity, and 0.5-mV maximum zero offset. Maximum temperature specifications include 30 ppm/°C linearity drift, 15 ppm/°C offset drift, and 400 ppm/°C gain drift. The specified operating case-temperature range is −25°C to +85°C.

Dynamic specifications for the AD9702 include voltage settling time, to ±3.2% gray scale, of 5 ns with ECL inputs and 6 ns with TTL, 3-nanosecond rise time, and glitch impulse of 80 mV-ns. The AD9702 can drive 75-ohm loads directly. ▶
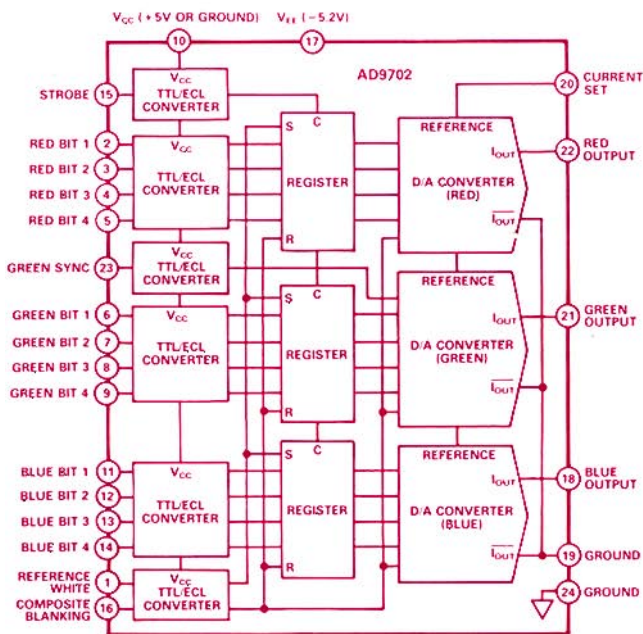

Figure 1. Functional bLock diagram of the AD9702.

*Use the reply card for technical data.

[1] For further information on glitches, consult the *Analog-Digital Conversion Handbook*, Third Edition, D. H. Sheingold, ed., Englewood Cliffs NJ: Prentice-Hall, 1986.

TESTING ENGINE EMISSIONS MORE EFFECTIVELY
MACSYM Automates Engine Testing, Increases Throughput And Precision
Example: Smoke Testing of Diesel Engines to EPA Standards by Onan Corp.

Tom Engman*

Automated product-test procedures improve data quality and save time and money. A computer-based test system can be used to both acquire and analyze data and to generate control signals to other piece of equipment used in the test. Most important, a computer system can deliver accurate repeatable data and analyze it to produce information that is meaningful to the test engineer.

Onan Corp., a prominent engine manufacturer, has recognized the importance of computer automation in effective engine testing—and of choosing a system which can be adapted to meet changing needs, especially where new products are evolving rapidly or testing procedures are likely to change.

To test diesel engines used in heavy-duty vehicular applications, Onan must follow detailed procedures outlined by the Environmental Protection Agency (EPA), in addition to other standard development test procedures.

EPA Test Requirements: Diesel engines manufactured by Onan are required to undergo two standard test procedures specified by EPA: the transient smoke test, which measures the opacity of diesel exhaust, and a transient gaseous emissions test, which determines the presence of pollutant gases such as carbon monoxide. Onan's capacity for in-house transient smoke testing has been greatly increased by computerizing of an existing test cell.

In automated test, engines are placed in specially designed test cells and instrumented with standard pressure transducers, thermocouples, and resistance temperature detectors (RTDs). Additional sensors measure parameters such as rpm, fuel consumption, and other parameters needed for special testing. The signals are carried outside the test cell via shielded cabling, which is hard-wired to the signal-conditioning inputs of the measurement-and-control system (Figure 1).
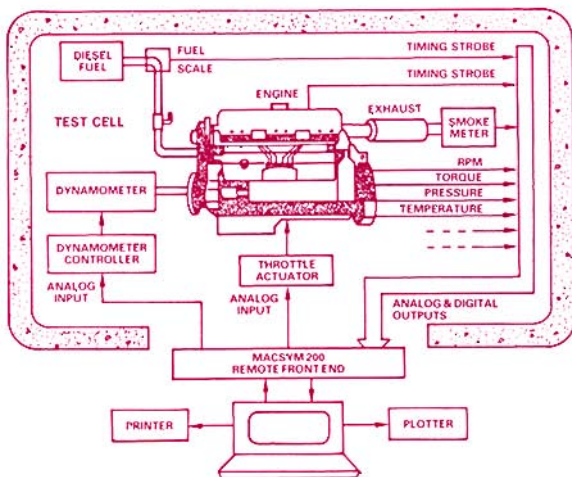

Figure 1. Block diagram of a typical test-cell installation. Everything is inside the cell except for the MACSYM system and peripherals.

The basic procedure for the transient smoke test—or *smoke opacity* test—consists of capturing the engine exhaust from the silencer, running it through a light-extinction smokemeter, and finally disposing of it through an exhaust hood. The smokemeter is positioned at the end of the exhaust pipe; a built-in light beam's intensity is modulated as the exhaust smoke plume passes by.

The smoke test requires a series of ramps and steady speeds or loads (Figures 2 and 3). Before the test begins, the engine must be run for 10 minutes at rated power. After the engine is conditioned in this way, it idles for five minutes, then three transient cycles are run and data is collected. The EPA requires three successful cycles for valid data; however if more than six tries are required, the engine must be reconditioned and the test must be re-started. Since reconditioning is a relatively lengthy process, it is highly desirable that it be made unnecessary. By accurately controlling the dynamometer to stay within the procedural test limits, Onan's automated procedure has all but eliminated the need to recondition.
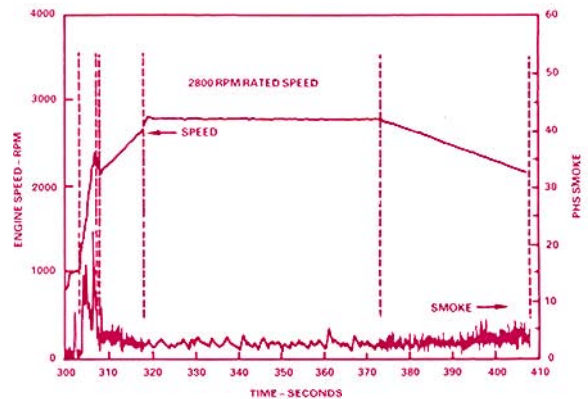

Figure 2. Smoke opacity data is analyzed during a series of acceleration ramps and steady speeds. This rpm and smoke vs. time plot shows speed and exhaust smoke data for a complete test cycle.

During the smoke test, the computer records exhaust gas opacity, engine rpm, and the precise time at which each data point is taken. Data is grouped into 0.5-second intervals and analyzed to determine the average smoke in each 0.5-second period. The conclusions of the test are three average values, A, B, and C, which are compared with standard values. A, B, and C are computed with algorithms prescribed by the EPA. To determine "A"—the average smoke reading during each 0.5-second interval—the computer must average 45 readings, which represent the 15 highest 0.5-second readings during the acceleration mode of each dynamometer cycle. Next, it determines "B" by averaging the 15 readings which represent the five highest 0.5-second readings during the lugging mode of each of three dynamometer cycles. Finally, "C" is determined as the average of nine readings representing the three highest values for each of three dynamometer cycles. If any value is inconsistent with the EPA standards, the test operator can make certain adjustments to alter the engine's performance and then rerun the test.
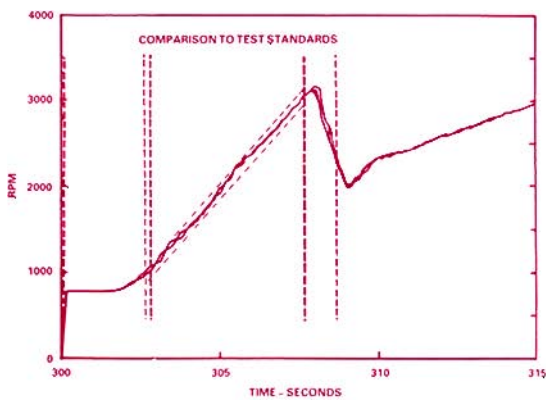
Figure 3. Plot of acceleration portion of the test with acceptability bands for speed variation.

The System: Onan chose the Analog Devices MACSYM 350 system†. The system's number-crunching capabilities, flexibility, multitasking operating system, comprehensive input/output (I/O) capability, and powerful software were important considerations. The MACSYM 350 system consists of a MACSYM 150 workstation, a MACSYM 200 remote front end, and a family of plug-in analog and digital I/O cards.

The system justified itself by increasing Onan's test capabilities and supplying a better log of data. The MACSYM system could perform in 20 minutes a test which might take 2-4 hours if performed manually, thus increasing Onan's testing capacity. Typically, six transient smoke runs can be completed in a morning; the resulting stored data from different tests can be compared with a single keystroke. Because of the system's ability to control the test parameters, repeatability on acceleration ramps is excellent—a difficult quality to achieve.

The conversion to an automated system took very little hardware modification. An existing steady-state test cell with existing equipment was automated by, in effect, adding the computer and hooking-up the sensors. The MACSYM's I/O capability was essential, because the application called for interfacing to a variety of signals. I/O cards for temperature, strain, torque, digital signals, pressure, frequency, and interrupts were among those used.

In this type of test application, the software considerations depend on the type of instrumentation used as well as the control algorithms, data-acquisition requirements, and desired data analysis for a given application. Onan needed real-time measurements of exhaust composition and engine parameters. To accurately characterize the process while it is happening, the computer must be able to sample I/O faster than the process parameters are changing. Since Onan needed about 60-120 samples per second, MACSYM's sampling speed (typically several thousand measurements per second) was more than adequate. The sample rate was especially important in the smoke test, where the minimum sampling frequency was 24 samples per second. Sampling rates of 60-80 samples per second bred increased confidence in the data.

The entire test is run from the keyboard of the MACSYM system; the operator need not activate any of the equipment manually. For example, certain values, such as the rated rpm, torque, and throttle position, are either typed in by the operator or—for a standard test cycle—entered automatically from disk.

†Use the reply card for technical data.

The computer controls test parameters, analyzes data, and performs statistical analysis; it linearizes instrument calibration data for each test and converts analyzer voltages to concentration levels. Accurately controllable eddy-current dynamometers load the engine, using controller setpoints provided by the MACSYM system.

The automated test system provides data which can immediately reveal the results of engine developmental changes through screen displays, printouts, and multicolor plots tailored to specific test requirements. The test operators can perform advanced analyses or prepare for the next test while the computer automatically implements the test procedure.

All values collected during the transient smoke test are saved on disk for future reference. Two parameters measured during this test—rpm and smoke opacity—plus the exact time, are collectively called a "data point." The test generates approximately 30 data points every 0.5 seconds—or around 120 external samples per second. A 10-megabyte hard disk accommodates the large volume of data generated by these test procedures. Then, if desired, color plots can be generated of each test to examine the differences between several test cycles, or to compare a test cycle to the standard. This provides a clear illustration of engine performance and helps technicians see where adjustments ought to be made.

MACBASIC The choice of a programming language was an important one. Onan's software was written in approximately one month using MACSYM's programming language, MACBASIC, developed by Analog Devices specifically for real-time measurement and control.

MACBASIC's multitasking feature was especially useful to Onan, simplifying programming of the engine test procedure, which involves several simultaneous operations. The program for the transient smoke test is made up of three tasks. *Task #1 controls the test* and comprises about two-thirds of the total program (about 200 lines of code). This task first sets up the test parameters, then sends control signals to the test cell to put the engine through its schedule of ramping, loading, and data analysis. While Task #1 is running, *Task #2 performs data acquisition*—taking readings from each transducer 30 times each 0.5 second, performing signal conditioning, and recording values. *Task #3 is for display*, which provides on-line graphics, updated twice per second. The program is written to give all tasks access to data collected by other tasks. This is an important function, because Task #1 needs rpm data collected by Task #2 in order to implement control functions, and Task #3 displays data from the other two tasks.

Because some tasks are more important than others, they can be assigned priorities or frequencies to ensure that they are performed often enough. In the smoke-test program, the control task includes the most time-critical functions; it was activated almost continuously. Next in priority was the data-acquisition task, while the display task had the lowest activation rate, twice per second.

MACBASIC includes specific integrated I/O commands, or "keywords," to make the programmer's job easier and provide rapid access to real-world analog and digital input and output. For example, the instruction, $Y = 4.2 * AIN (3,2)$, converts the conditioned input signal at channel 2 of the card in slot 3 of the MACSYM 200 to digital, multiplies it by 4.2, and assigns it the variable, Y, all in considerably less than 1 millisecond. ▶

# FOUR NEW MONOLITHIC CMOS ANALOG-TO-DIGITAL CONVERTERS

AD7578: 12 Bits, 100 μs
24-Pin 0.3" "Skinny" DIP
No Missed Codes over Temp
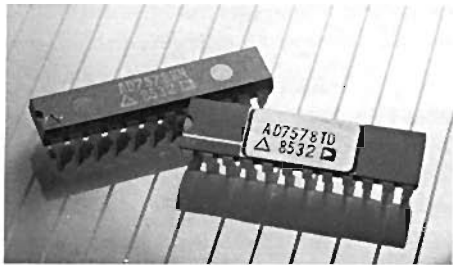
The AD7578* is a 12-bit monolithic CMOS a/d converter (ADC) packaged in a 0.3" narrow 24-pin DIP. Maximum total unadjusted error (including gain, offset, and linearity errors) is ±1 LSB maximum over the full operating temperature range—and the user can choose among three ranges: the plastic AD7578KN (0°C to +70°C), the ceramic BD (−25°C to +85°C), and the ceramic TD (−55°C to 125°C). Prices start at $19.95 (100s).

Applications include telecommunications, avionics control, high-performance modems, and remote applications that require the low power (75 mW) inherent in CMOS, small size, high precision, and "no tweaks" (¼-LSB max gain & offset errors).

Its high-impedance analog input is free from the problems of source loading found in many ADCs. The successive-approximation conversion employs either an internal or an external clock. Right-justified output data is available on an 8-bit bus in two bytes, 4 MSBs and 8 LSBs, in either order. ▶
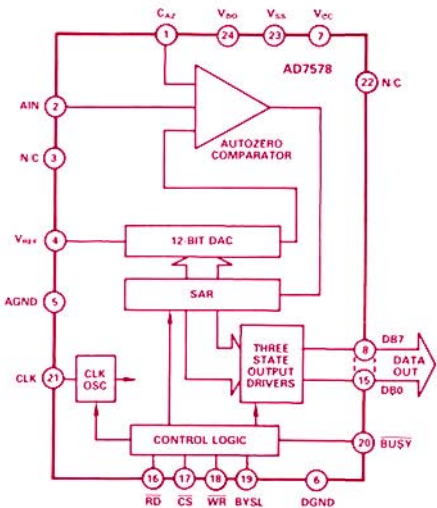
4-, 8-Channel, 2.5-μs 8-Bit A/D Converters
AD7824 & AD7828 Have Track/Hold, Multiplexer
½-LSB max Total Unadjusted Error (L,C,U Versions)

The AD7824 and AD7828* are high-speed, multi-channel 8-bit ADCs with a respective choice of 4 or 8 multiplexed analog inputs. A dual-4-bit-flash subranging a/d conversion technique ("half-flash") gives a fast conversion time of 2.5 μs per channel (400,000 conversions per second) for both types.

The basic converter is similar to that of the AD7820, recently introduced in this Journal (19-1, 1985, p.15). Total unadjusted error is less than ±½LSB (L,C,U grades) or ±1LSB (K,B,T grades).

An on-chip track/hold function with 157 mV/μs slewing rate permits full-scale signals of up to 10kHz to be digitized, but complex signals may contain small components up to the respective Nyquist frequencies of 50kHz (4 channels) or 25kHz (8 channels) per channel—or even higher if channels are sampled more frequently at uniform intervals. This greatly simplifies the design of anti-aliasing filters.
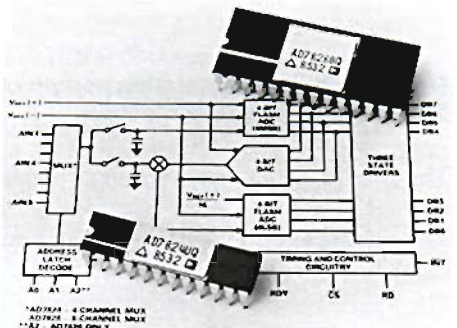
Both devices operate from single +5-volt supplies and have an analog input range of 0 to +5V, using external 5-V references. Both interface to μPs, using Chip-Select and Read signals to select input channels, initiate conversions, and read data from the 3-state outputs. The AD7824 and AD7828 are housed in 0.3"/24-pin and 0.6"/28-pin DIPs. All standard temperature ranges are available. Prices start at $10.45 (100s). ▶

AD7575: 8-Bit, 5-μs Sampling ADC Has on-Chip Track/Hold
Housed in 0.3" 18-Pin Plastic or Ceramic DIP
±1-LSB Total Unadjusted Error (K,B,T Versions)

The AD7575* is a low-cost 8-bit ratiometric CMOS a/d converter with an on-chip track-and-hold function; it performs a complete conversion in 5 μs (sampling rates to 200kHz), while its T/H's 386 mV/μs slewing rate allows 50-kHz full-scale sinusoidal signals to be digitized; signal-to-noise is 45 dB with a 10-kHz signal, 4 dB (2/3 LSB) below 8-bit theoretical.

The device uses a single +5-volt supply; with a low-cost 1.23-volt bandgap reference—such as the AD589*—it can convert signals from 0 to 2 V_{REF}. Total unadjusted error—including T/H and linearity-, gain-, and zero errors of the ADC—amounts to less than ±1LSB over temperature for AD7575K/B/T (3 temperature ranges) and ±2LSB max for J/A/S versions. Prices (100s) start at $5.50 (JN: 18-pin plastic DIP).

Besides being accurate, low in cost, fully specified, and easy to use, it has low power consumption—35 mW max. Compatible

with all popular μPs, it combines short conversion time and fast bus interface times—100ns bus access, 10ns bus relinquish, and Read pulse-widths of 100ns.
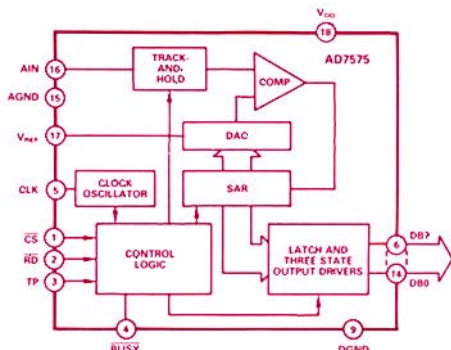
Most effectively used in high-frequency sampling, it is ideally suited for applications in simultaneous converter-per-channel sampling of multiple channels, e.g., phased-array sonar. Other application areas include geophones, disk drives, modems, and medical ultrasonics. ▶


*Use the reply card for technical data.

FOUR HIGH-SPEED 12-BIT ANALOG-TO-DIGITAL CONVERTERS

CAV-1202: 12-Bit, 2-MHz ADC on Eurocard
Complete with Track/Hold and Timing Circuitry
High-Resolution Conversion at up to 2-MHz Sampling Rates

Improved HAS-1202
1.56 µs, 12-Bit Hybrid
High Speed, Low Price

The CAV-1202* is a complete 12-bit, 2-MHz sampling analog-to-digital converter, including a track-and-hold amplifier, constructed on a board measuring 167.30 × 100.00 × 13.13-mm (6.59″ × 3.93″ × 0.517″)—including connectors. Based on the Level 2 requirements for printed-circuit subunits, the design meets the standards established by DIN 41494, IEC 48D (sec) 12 for assemblies based on the standardized 19″ system employing Europa and double-Europa sized printed circuit boards.

With all timing circuits and the T/H on board, the CAV-1202 needs only an Encode command and external power supplies (± 15V, + 5V, and − 5.2V). The converter is used in applications calling for high sample rates, such as transient analysis, radar digitizing, and medical instrumentation.

Full-scale analog input is ± 2.048V (1mV per bit), and the parallel 12-bit output is TTL-compatible. Two-step subranging, with digital error-correction, provides
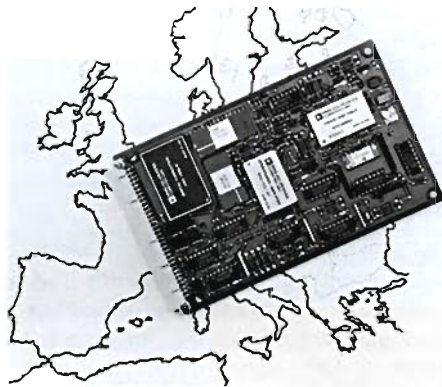
monotonic operation over temperature, 0°C to +70°C. Low-frequency error totals 0.012% of full scale, including nonlinearity.

Spurious in-band signals generated at a 2-MHz encode rate are typically 74dB below full scale for input signals from dc to 500kHz and − 67dB from 500kHz to 1MHz. Typical signal-to-noise is 66dB at 360kHz. Price (1's) is $1,940. ▶
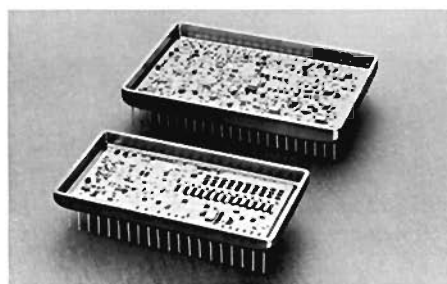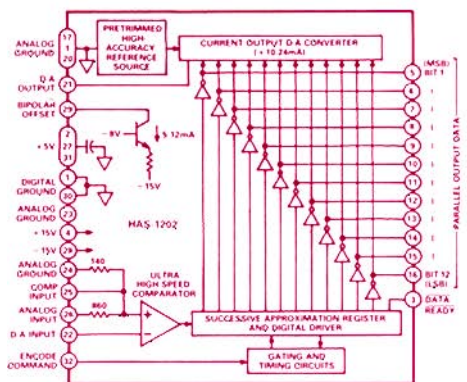
The HAS-1202A* is a complete, fast hybrid 12-bit a/d converter, pin-compatible with the venerable HAS-1202, announced in these pages in 1979 (*Analog Dialogue* 13-2). Since then, the HAS-1202, with its 349-kHz max conversion rate, has been teamed up with the HTC-0300A track-hold for high-speed digitizing in a great many applications.

They have found sockets in radar systems, PCM, digital signal-processing (DSP), and data acquisition for systems that are used in such real-world applications as gamma-ray cameras, waveform analysis, and lumber-grading systems.

Since users always need more speed, the HAS-1202A, with its maximum conversion rate of 641kHz—nearly double that of HAS-1202—has been developed to permit systems with HAS-1202 sockets to be easily upgraded to word rates in excess of 550kHz.

The HAS-1202A's other specifications are identical to those of the HAS-1202. Both are packaged in 32-pin ceramic DIPs for 0°C to +70°C operation—and hermetically sealed metal cans, for − 25°C to + 85°C—and − 55°C to + 100°C—operation. Prices start at $175 in 100s. ▶

Two 12-Bit Hybrids with Internal Track/Holds
1-MHz HAS-1201: 46-Pin Hermetic Metal Package
500-kHz HAS-1204: Complete in a 40-Pin Metal DIP

The HAS-1201* and HAS-1204* are 12-bit hybrid a/d converters with on-board track-holds for sampling conversion. The HAS-1201 can convert at rates up to 1MHz, while the HAS-1204 converts at up to 500kHz.

They incorporate T/H, a/d converter, and timing circuits; to operate, they need only an encode command and power. The HAS-1204 is jumper-programmed for (unipolar or bipolar) 5-V or 10-V full-scale input and requires 2.2 watts of power at ± 15 volts and + 5 volts. The HAS-1201 (3 watts) needs the same voltages, plus a − 5.2-volt supply; it too can handle bipolar or unipolar 5- or 10-volt full-scale inputs.

The table outlines typical dynamic performance for the two devices.

Both devices are housed in hermetically sealed metal packages. The HAS-1201 is avail-

	HAS-1201	HAS-1204
In-band harmonics	− 80dB	− 75dB
Signal/Noise	68dB	69dB
for input:	100kHz	50kHz
Input bandwidth large signal	2MHz	4MHz

able for 0°C to +70°C and − 25°C to +85°C operation (case temperatures); the HAS-1204 has − 25°C to +85°C and − 55°C to + 100°C grades. Prices for the HAS-1201 and HAS-1204 (100s) start at $395 and $294. ▶

*Use the reply card for technical data.

MONOLITHIC AD574A
Lowest Cost in Plastic
Highest Reliability in Ceramic
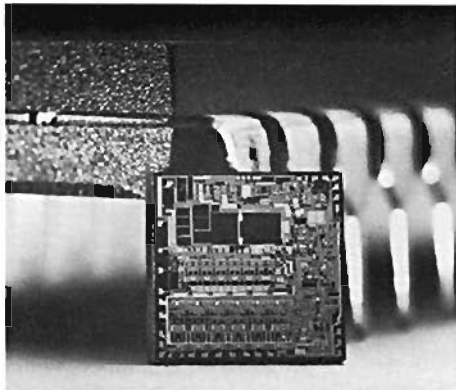
For the first time, the industry-standard AD574 12-bit a/d converter (*Analog Dialogue* 12-3, 1978, page 3) is available in a single-chip version. The new monolithic AD574A* is available in plastic packaging at the lowest known AD574 price: only $27.90 in 100s (J version).

Packaged in a 28-pin DIP, the AD574A is also available with MIL-STD-883C, Class B, processing for military and other high-rel applications. Pricing in 100s for *ceramic-packaged* parts starts at $30.65.

Because of its high resolution, low price and ease of use, AD574 appears in a great many general-purpose data-acquisition applications. The monolithic AD574A includes a microprocessor interface, clock, and reference on one chip. A drop-in replacement for its two-chip predecessor, it retains the same pinout and performance.

The converter features 3-state output buffers for direct interface with 8-, 12-, or 16-bit buses, and a 250-ns bus-access time. Its internal reference is trimmed to 10.00V, and 4 calibrated input voltage ranges are available, 0 to +10V or +20V, ±5V, and ±10V.

Operating from +5V and ±12V or ±15V supplies, the AD574A is specified from 0° to +70°C for the J, K, and L grades, and from −55°C to +125°C for the S, T, and U grades. Conversion time is 35 μs and dissipation is 725 mW max. Grades K/L/T/U guarantee maximum linearity error of ±½ LSB (±0.01%) and no missing codes (NMC) over temperature; grades J/S guarantee maximum linearity error of ±1 LSB and NMC to 11 bits over temperature. ▶
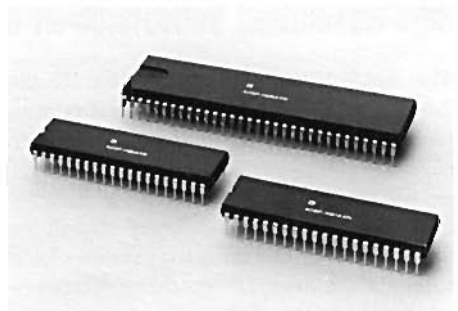
*Use the reply card for technical data.

3 FAST 1.5-μm CMOS DSP CHIPS
ADSP-1009A: 70-ns 12 × 12-Bit CMOS Multiplier/Accumulator
Two 8 × 8-Bit 30-MHz Multipliers: Twos-Complement & Unsigned

Since the introduction in 1982-83 (*Analog Dialogue* 17-1) of our CMOS DSP chips as low-dissipation replacements for standard high-wattage bipolar multipliers and MACs, we have developed a 1.5-μm process to succeed the original 5-μm process; this gives increased speed and makes possible new, more-complex, proprietary chip designs. You have already encountered some of these in pages 7-11.

The new process is also used to produce higher-speed replacements for the earlier multipliers and MACs. For example, in *Dialogue* 18-3 (p.18), we introduced the ADSP-1016A*, ADSP-1010A*, and ADSP-1008A*; all were at least twice as fast as their 5-micron counterparts.

They are now joined by the ADSP-1009A 12×12 Multiplier/Accumulator* (70ns), the ADSP-1080A 8×8 Twos-Complement Multiplier* (33ns), and the ADSP-1081A 8×8 Unsigned-Magnitude Multiplier* (33ns). Each is fully pin-compatible with its predecessor and at least twice as fast; low-cost plastic versions are available. Prices (100s) start at $27 for the 8-bit devices and $53.30 for the 12-bit ADSP-1009AN.

8- and 12-bit multipliers and MACs are particularly popular in video, imaging, radar, and telecommunications, where 16 bits is overkill, and higher speed and two output ports give higher throughput. Applications also include 2-dimensional image filtering, graphics transformations, TV special effects, and high-speed modems. ▶

# MIL-TEMP VERSION OF AD578 A/D CONVERTER
12 Bits in 4.5μs Guaranteed (T Version)
No Missing Codes over Temperature

The AD578SD and AD578TD* are wide-temperature-range versions of the AD578 high-speed 12-bit hybrid ADC, which has more than 5 years of production experience (*Dialogue* 14-2). Assembled in hermetically sealed 32-pin side-brazed ceramic DIPs, they are functionally complete, including reference and clock. They are designed for applications requiring operation over the MIL-temperature range, −55°C to +125°C.

The AD578TD and AD578SD perform complete 12-bit conversions within 4.5μs and 6.0μs maximum, are tested to have no missing codes over the entire operating temperature range, and operate with power supplies of +5 volts and either ±15 volts or ±12 volts (Z grade); they dissipate only 875 mW.

Use them in high-speed data-acquisition, with throughput rates up to 222kHz, radar/sonar signal processing, electronic countermeasures, and seismic equipment. Prices (S/T) are $165 and $205 in 100s. ▶
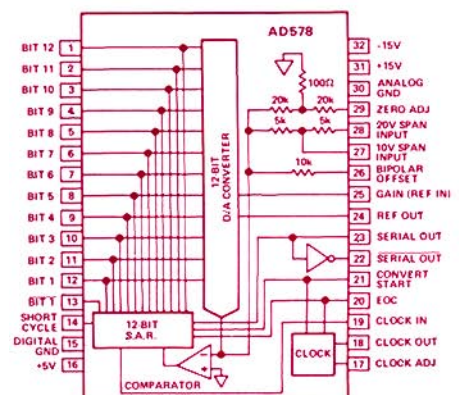
TRIPLE DAC FOR RASTER-SCAN GRAPHICS
HDL-3805/3806: 3 Fast 8-Bit DACs with Lookup Tables
## 85-MHz Writing Rate with 12-ns Settling Time

The HDL-3805 and HDL-3806* consist of three 8-bit video DACs and three 256×8 ECL random-access-memory lookup tables (LUTs) in a single hybrid package. Settling time of the DACs is 12 ns; minimum top update rates are 115 MHz for the latched HDL-3806, 85 MHz for the asynchronous HDL-3805. Prices (100s) start at $335.

Replacing 3 DACs and 3 LUTs in raster-scan display systems, the small RGB (red
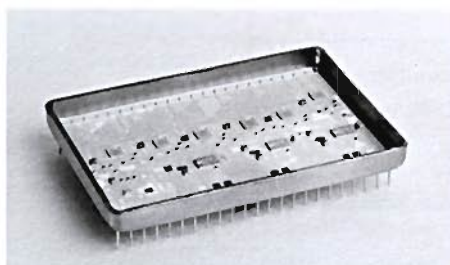
green blue) video generator can save board space and improve reliability over discrete approaches. The devices are also useful in other applications requiring multiple DACs with ultra-fast output settling.

8 bits of gray-scale resolution per channel give the user a palette of 16.7 million available color combinations. On each sweep, a total of 256 colors is available; and the write speed of the RAMs is sufficiently high to rewrite the color map completely during the vertical retrace—or update smaller blocks of data during the horizontal retrace. ▶
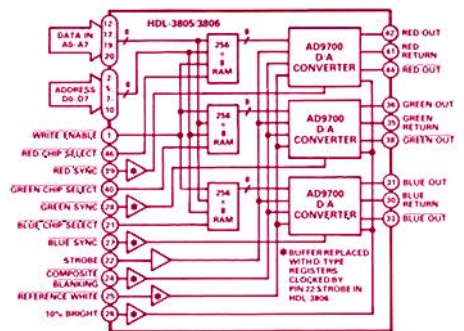
TTL-COMPATIBLE DACS FOR RASTER DISPLAYS
8-Bit HDG-0807 & 4-Bit HDG-0407: Single-Supply Operation
Complete Composite Controls; HDG Series Pin-Compatibility

The HDG-0807 and HDG-0407* 8- and 4-bit raster-scan d/a converters add another capability to the HDG family of complete raster DACs (*Analog Dialogue* 15-2, pp. 3-6 and 19-1, p. 22), i.e., they are compatible with TTL-level signals and need only a single +5-volt power supply to generate standard video levels referenced to ground.
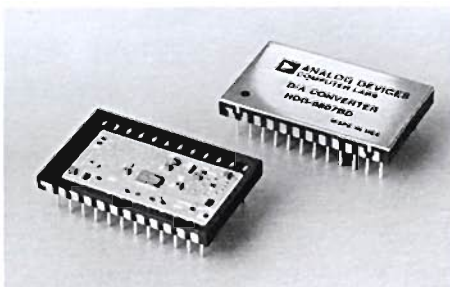
They avoid the necessity for translating from TTL to ECL for users who must work with TTL signals. Like the original HDG Series, the new units have complete, asynchronous (synchronous optional) composite controls, including self-contained digitally controlled sync and blanking, and a reference-white control input—as well as a 10% enhanced brightness capability.
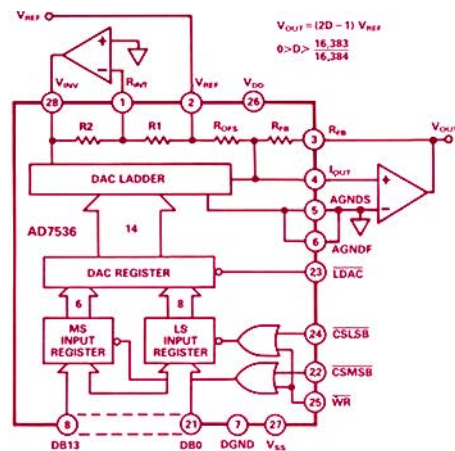
The devices have internal references, 14-ns settling time and 50-MHz update rate (8-bits), operate at temperatures from $-25°C$ to $+85°C$, dissipate 1.125 W, and are of hybrid construction (24-pin DIP). Prices (100s, 8 bits) start at $43. ▶
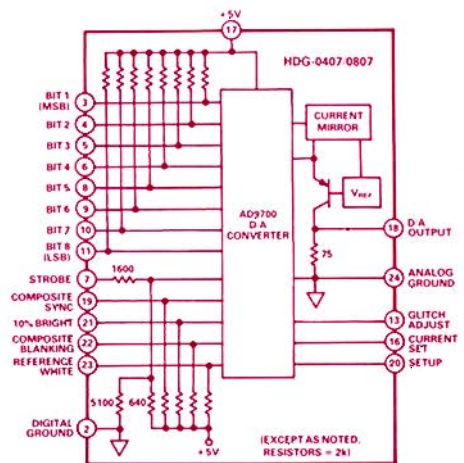
14-BIT M-DAC
AD7536: No External Resistors
For 4-Quadrant Operation

The AD7536* is a 14-bit monolithic CMOS 4-quadrant multiplying d/a converter with all resistors needed to provide accurate four-quadrant multiplication when connected to a pair of external op amps. It can be thought of as either a bipolar d/a converter with the full range of positive or negative reference voltages, or as a digitally programmed attenuator of full-range positive-to-negative analog signals (gains of either polarity).

It is a high-accuracy device: all grades are guaranteed 14-bit monotonic over temperature; and integral nonlinearity (relative-accuracy error) is less than $\pm 1 LSB$ max over temperature for grades K/B/T—and only $\pm 2 LSB$ max for grades J/A/S. Output leakage current is less than 20nA over the full temperature range. Current settling time is typically $0.8 \mu s$. Prices start at $18.95 in 100s.

Typical applications include μP-based control systems in high-temperature environments, digital audio systems, precision servo control loops, and high-performance, high-resolution military applications.

It is easy to use from both the analog and digital points of view. Its flexible double-buffered latch structure permits (right-justified) interfacing, either broadside on 16-bit data buses or in two bytes (6-8) on 8-bit buses. It can be used for 4-quadrant multiplication without any external resistors. And the chip's ground configuration permits the device's analog ground to be sensed, compared with system signal ground, and forced to follow accurately using an external op amp. ▶

*Use the reply card for technical data.

Worth Reading

All publications listed here, are available free upon request, *except for any marked with an asterisk (*)*. Use the reply card or get in touch with Analog Devices or the nearest sales office.

Analog Briefings

This is a newsletter published by Analog Devices for the military/avionics industry. In the latest issue, Volume 1, Number 2 (October, 1985), topics include: MIL-STD-1772 certification of hybrid facilities at our Microelectronics Division; monolithic version of the AD574A; MIL-STD-883C and "grandfathered" spec-control drawings; hybrid DAC87, DESC drawing 8300201JC (DAC87), and monolithic DAC87, DESC drawing 8300301JA; *Military Products Databook* errata. To receive *Analog Briefings* regularly, get in touch with the nearest ADI sales office or representative.

Application Notes

Curtin, Mike, "Interfacing the AD7549 Dual Monolithic 12-Bit DAC to the MCS-48 and MCS-51 Microcomputer Families" (4 pages).

Gasking, John, "Resolver-to-Digital Conversion—a Simple and Cost-Effective Alternative to Optical Shaft Encoders" (4 pages).

Jung, Walt, "AD670 8-Bit A/D Converter Applications". Discusses signal-conditioning applications for an 8-bit a/d converter with a built-in instrumentation-amplifier front end (12 pages), by the author of *IC Op-Amp Cookbook*.

————, "Applying IC Sample-Hold Amplifiers" (8 pages). Includes: basics; errors in Sample, Hold, and transitions, dielectric absorption, drift and noise, design types, applications.

————, "Operation and Applications of the AD654 IC V-to-F Converter" (28 pages, with references). Includes: description; theory; basic operational modes; timing-component considerations; plus some 26 application topics and 28 cookbook-type figures.

Kitchin, Charles, Andrew Wheeler, and Ken Weigel, "Low-Cost Two-Chip Voltage-Controlled Amplifier and Video Switch". Employs the AD539 dual-channel wideband (60MHz) analog multiplier (6 pages).

Klonowski, Paul, "Use of the AD590 Temperature Transducer in a Remote Sensing Application". Transmitting an AD590 temperature signal 1000 feet with negligible loss of accuracy (4 pages).

Nickson, Paul, "Dynamic Resolution Switching on the 1S74 Resolver-to-Digital Converter" (2 pages).

————, "Why the Velocity Output on the 1S74 and 1S64 Series Converters is Continuous and Step-Free Down to Zero Speed" (2 pages).

Reidy, John, "10-Bit-Resolution Temperature-Measurement System Using the AD7571 [10-bit + sign CMOS ADC] and the AD594/595 [cold-junction compensated thermocouple preamp] (4 pages).

Wynne, John, "AD7224 Provides Programmable Voltages over Varying Ranges" (4 pages).

————, "Simple Interface Between D/A Converter and Microcomputer Leads to Programmable Sine-Wave Oscillator" (6 pages).

————, "Generate 4 Channels of Analog Output with AD7542 12-Bit D/A Converters, and Control It All with Only Two Wires" (6 pages).

Brief Book* Review

Schweber, W.L., *Integrated Circuits for Computers: Principles and Applications*. New York: McGraw-Hill Book Company (1986). An excellent 408-page introductory text—with many exercises. Covers ICs, SSI, gates, decoders, multiplexers, buffers, ALUs, major IC families, memory ICs, support ICs, analog interface, μPs, and test equipment & methods. Practical orientation; easy to read; aimed at students; no advanced math. [*Not available from Analog Devices.*]

Brochures

Applications Guide for Isolators and Signal Conditioners (20-page December, 1985 edition—includes AD202/AD204).

Data-Conversion Integrated Circuits Selection Guide to ICs and hybrid circuits from Analog Devices (32 pages, 16 charts).

Temperature Meters with a Difference. AD2050/51 and AD2070/71 thermocouple meters and AD2060/61 RTD-Thermistor meter (2 pages).

Reprint of Article by ADI Author

Boyes, Geoff, "Sensor, ADC Specs Set Angular-Measurement Systems' Performance," *EDN*, January 24, 1985. ▶

MORE ADI AUTHORS *(Continued from page 2)*

James Conant (page 3) is a Senior Marketing Engineer in the Interface Products Division of Analog Devices. Since joining ADI in 1969, he has held positions as a Test-equipment Design Engineer and Senior Product Engineer. In his most recent position as Senior Applications Engineer, he presented technical seminars in Australia, Japan and the People's Republic of China. He is a member of both ISA and ISHM.

Donald W. Brockman (page 17) is Technical Communications Manager at ADI's Computer Labs Division (formerly Computer Labs Incorporated), which he joined in 1968 from Bell Telephone Laboratories. His formal education includes a B.A. degree and he has worked in engineering, writing, recruiting, and sales functions before his present job in Marketing.

Ed Garibian (page 16) is a Marketing Engineer at ADI's Microelectronics Division, in Wilmington, Mass. He earned a BSEE from the University of Massachusetts, Amherst. Before he joined Analog Devices, he was a Design Engineer for Texas Instruments, in Dallas. ▶

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and
Topical Interest. Further Information on Products
Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE (Volume 19, Number 1, 1985 -- 28 pages):
   Complete Monolithic Analog Multifunction Chip, Output = Z(Y/X)^M [AD538]
   Dual 12-Bit CMOS Microprocessor-Compatible DAC in 0.3" DIP [AD7549]
   24 X 24-Bit Fixed-Point CMOS Digital Multiplier [ADSP-1024]
   Low-Cost Voltage-to-Frequency Converter Chip [AD654]
   High-Performance Precision Hybrid Isolation Amplifier [AD295]
   New Plug-In Signal-Conditioning Modules for 3B Series [3B47, 3B17]
   Double-Buffered 14-Bit Monolithic CMOS Multiplying DAC [AD7535]
   Low-Cost 8-Bit Monolithic ADC Converts in 1.36 us Max [AD7820]
   Software-Programmable-Gain Amplifier-Track/Hold for Data Acquisition [AD365]
   High Performance 10-Bit, 800-ns A/D Converter [AD ADC-816]
   Real-World I/O Cards for the CMOS STD Bus [RTI-1280/1281/1282]
   Thermometer with Resolution Better than 0.0001°C
   New-Product Briefs: . . . Fast 8-Bit Monolithic CMOS ADC Converts in 10 us [AD7576] . . . Low-Cost 12-Bit Resolver-to-Digital
Converter [2S20] . . . New Options in HDG 4-to-8-Bit Raster DAC Family . . . Thermocouple Amplifiers in Cerdip for Types J and K
[AD549Q/595Q] . . . Precision BiFET Op Amps in Metal and Cerdip [AD611] . . . Precision Op Amp with Existing Second Sources
[AD OP-37] . . . 16-Bit Hybrid A/D Converter -- 17 us Max Conversion Time [AD376] . . . Digital-to-Resolver/Synchro Transformers
-- Low Profile, Low-Frequency . . . Hi-Rel for Non-Military Parts -- Analog Devices PLUS program.
   Worth Reading: Review of Prentice-Hall's new ANALOG-DIGITAL CONVERSION HANDBOOK, 3rd edition, by the Engineering Staff of Analog
Devices, Edited by Daniel H. Sheingold (1986). Available from Analog Devices at $32.95 postpaid. Send check to P.O. Box 796, Norwood
MA 02062, or phone VISA information to (617)-461-3392 . . . List of new free publications from Analog Devices . . . List of References
for High-Resolution Thermometer Article.
   Editor's Notes, Analog Devices Authors, Promotion of Peter Holloway to Division Fellow, Potpourri, Advertisement: "Evolution of the
total 12-bit DAC." [AD667]

PRODUCT NOTES . . . Zero offset-adjustment: Bipolar d/a converters using 1/2-scale offset (and usually offset-binary coding) are
zeroed at all-zeros (-full scale); and their span is adjusted at all-ones (+full scale - 1 LSB). This may result in an offset from
analog zero at mid-scale (10000...00). If such offsets are critical, the zero may be readjusted at mid-scale by either offsetting the
DAC's output amplifier or introducing a balancing dc offset into the system's signal path - either manually or with a low-resolution
trim DAC . . . AD376KM spec change: Unipolar offset drift is 4 ppm/°C . . . AD639 Monolithic Trig-Function Generator supply range:
minimum recommended supply-voltage range for standard units over industrial and military temperature ranges is +6 volts . . .
There's a better way to zero the Model 289 Isolation Amplifier for low-resistance loads (2 to 25k ohms) than is shown in Figure 5B
of the data sheet: Zero-adjust at the input, using a 25-k pot across $\pm V_{iso}$ (pins 2-3), with the tap connected to pin 4 (Gain) in
series with a 4.99-megohm resistor. The small (0.2%) resulting gain error can be compensated for (if necessary) elsewhere in the
signal path. As an added benefit, the dual power supply required by Figure 5B can be eliminated . . . 2B50 Thermocouple Amplifier
open-thermocouple detection: for negative overscale, connect pin 39 to pin 2; for positive overscale, connect a 500-megohm resistor
between pin 8 and pin 2. Response time depends on gain, is about 1.4 s at G = 250 . . . AD293/AD294 Isolation Amplifiers,
new synchronizing scheme: connect 0.0015 uF in series with each amplifier's sync pin and tie the capacitors together. The
synchronizing frequency is determined by the isolator with the lowest carrier frequency; no external oscillator is necessary . . .
HTS-0025 Track/Hold power sequence: V_{CC}+ and V_{CC}- must be applied simultaneously with, or ahead of, V+ and V- 15-volt supplies .
. . Card-level video ADCs: If the Encode command signal source has high internal source resistance, an external 510-ohm terminating
resistor should be connected between Encode and -5.2 V . . . 1S64 & 1S74 Resolver-to-Digital Converters: For lowest offset when
implementing gains between 1 and 10 for the velocity output, R_{ext} should be connected to the "GROUND SENSE" pin (instead of GND); it
is located between the ANGLE OFFSET and INTER LSB pins. This feature is available on all but the earliest units in these series . . .
New Gain Error specs on AD7541AKN/ABQ/ATD 12-Bit CMOS D/A Converters: +3 LSB @ 25°C and +5 LSB, T_{MIN} to T_{MAX} . . . MACSYM 260
now has improved environmental specs. MACSYM 260 (and to a lesser extent, MACSYM 250) is available at substantially lower prices.

DATA SHEETS . . . AD7571 (10-bit CMOS ADC) has a new data sheet, with changes to the clock components (R_{CLK} = 56 k ohms,
C_{CLK} = 150 pF) and corrected serial data output specs: t_{SDS} = 500 ns min and t_{SDH} = 20 ns min. New data sheet number (on last
page along spine) is C763a-10-12/85 . . . ADLH0032 caution: Don't use the high-speed comparator circuit of Figure 3 on data sheet
C605a-3-5/82 . . . HDG-0407/0807 (raster DAC) data sheet C952-9-10/85: first Feature on page 1 should read "Update Rates to 50 MHz"
. . . HAS-1202/HAS-1202A (12-bit ADC) data sheet C938-9-9/85: in Specifications, page 2, Gain Error %FS (max) should read 0.08
(0.18). In Figure 1, move legends DATA READY and BIT 1 (MSB) up and BIT 12 (LSB) down to relate them to respective waveforms. In
Figures 3 and 4, blocks labeled HAS-1201/1202A should read HAS-1202/1202A . . . ADSHM-5/ADSHM-5K data sheet C612-9-1/81: There
should be only two horizontal grid lines (not 3) between pins 24 & 26 and pins 8 & 9. This is corrected in Databook . . .
AD7820 (8-bit ADC) Data Sheet C892-9-3/85: in Specifications, page 2, Units for Total Unadjusted Error should be LSB max.
Incidentally, your nearby ADI component sales engineer can show you a comparison table based on testing of AD7820 and one
manufacturer's ADC0820 with ten different microprocessors, with clock rates from 3.2 MHz to 12.5 MHz. AD7820 appears to acquit itself
quite favorably (for example, the AD7820 works over all temperature ranges with the 68008, with clocks from 8 to 12.5 MHz) . . .
AD7582 (CMOS ADC) old data sheets - on page 5, the Truth Table for the pin-function description of pins 24 and 25 should be headed:
A1 A0 (they had been reversed). The new corrected data sheet is C839b-10-7/85 . . . MOD-1020 (Video ADC) data sheet C554a-5-2/85 -
the five numbers listed under Power Requirements should be: 350(390), 250(280), 100(115), 2.8(3.1), 24(26.7).

RELIABILITY, ETC. . . . ADI's Microelectronics Division (MED), in Wilmington MA, has received certification of compliance to
MIL-STD-1772 from DESC (Defense Electronics Supply Center). The military standard specifies certification requirements for hybrid
manufacturing facilities . . . MED is now shipping ADDAC87CBI-V/ against DESC drawing 830020LJC; though not a JAN part, a device
conforming to the DESC drawing is qualified at a higher level than a standard commercial part with a /883 designation . . .
Electrostatic-Discharge (ESD) Protection: When handling ESD-sensitive parts - at any stage - it is imperative that a grounded work
station be used to prevent damage. Compact and inexpensive portable electronic work stations typically consist of a conductive vinyl
surface and pairs of wrist straps and ground leads; they are available from a number of suppliers, such as Charleswater Products,
Inc., 93 Border Street, West Newton MA 02165. Their cost is comparable to that of an average hardcover textbook . . . AD584 is now a
JAN part, the first precision voltage reference to be listed on DESC's qualified parts list (QPL - 38510). The full name of the
"S" grade is JM38510/12801BGC (the "T" grade's slash number is /12802BGC). Specifications of these products ("slash sheets") are
available from Naval Publishing and Forms Center, 5801 Tabor Avenue, Philadelphia PA 19120, (215) 697-3321 - not from Analog Devices.

NEW PATENTS ISSUED . . . 4,511,413 (Ralph C. Tuttle and Richard S. Payne) Process for Forming an IC Wafer with Buried Zener Diodes
. . . 4,521,764 (David P. Burton) Signal-Controllable Attenuator Employing a Digital-to-Analog Converter [LOGDAC^{TM}] . . .
4,543,560 (Peter R. Holloway) Two-Stage High Resolution Digital-to-Analog Converter [AD569] . . . 4,543,561 (Peter R. Holloway)
Single-Supply IC Digital-to-Analog Converter for Use with Microprocessors [AD558] . . . 4,547,766 and 4,556,870 (Adrian P. Brokaw and
Modesto A. Maidique) A-to-D Converter of the Successive-Approximation Type [AD571] . . . 4,547,961 (Delip R. Bokil and William H.
Morong III) Method of Manufacture of Miniaturized Transformer [AD293] . . . 4,558,242 (Michael G. Tuthill and Paschal Minogue)
Extended Reference Range Voltage-Mode CMOS D/A Converter . . . 4,562,400 (Tanjore R. Narasimhan) Temperature-Compensated Zener Voltage
Reference.